CD4046B Types

CMOS Micropower Phase-Locked Loop

■ CD4046B CMOS Micropower Phase-Locked Loop (PLL) consists of a low-power, linear voltage-controlled oscillator (VCO) and two different phase comparators having a common signal-input amplifier and a common comparator input. A 5.2-V zener diode is provided for supply regulation if necessary.

The CD4046B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

VCO Section

The VCO requires one external capacitor C1 and one or two external resistors (R1 or R1 and R2). Resistor R1 and capacitor C1 determine the frequency range of the VCO and resistor R2 enables the VCO to have a frequency offset if required. The high input impedance ($10^{12}\Omega$) of the VCO simplifies the design of low-pass filters by permitting the designer a wide choice of resistor-to-capacitor ratios. In order not to load the low-pass filter, a source-follower output of the VCO input voltage is provided at terminal 10 (DEMODULATED OUTPUT). If this terminal is used, a load resistor (R_S) of 10 kΩ or more should be connected from this terminal to V_{SS}. If unused this terminal should be left open. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. A full CMOS logic swing is available at the output of the VCO and allows direct coupling to CMOS frequency dividers such as the RCA-CD4024, CD4018, CD4020, CD4022, CD4029, and CD4059. One or more CD4018 (Presettable Divide-by-N Counter) or CD4029 (Presettable Up/Down Counter), or CD4059A (Programmable Divide-by-"N" Counter), together with the CD4046B (Phase-Locked Loop) can be used to build a micropower low-frequency synthesizer. A logic 0 on the INHIBIT input "enables" the VCO and the source follower, while a logic 1 "turns off" both to minimize stand-by power consumption.

Features:

■ Very low power consumption:
70 μW (typ.) at VCO f_o = 10 kHz, V_{DD} = 5 V
■ Operating frequency range up to 1.4 MHz (typ.) at V_{DD} = 10 V, RI = 5 kΩ
■ Low frequency drift: 0.04%/°C (typ.) at V_{DD} = 10 V
■ Choice of two phase comparators:
Exclusive-OR network (I)
Edge-controlled memory network with phase-pulse output for lock indication (II)
■ High VCO linearity: <1% (typ.) at V_{DD} = 10 V
■ VCO inhibit control for ON-OFF keying and ultra-low standby power consumption
■ Source-follower output of VCO control input (Demod. output)
■ Zener diode to assist supply regulation
■ Standardized, symmetrical output characteristics
■ 100% tested for quiescent current at 20 V
■ 5-V, 10-V, and 15-V parametric ratings
■ Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

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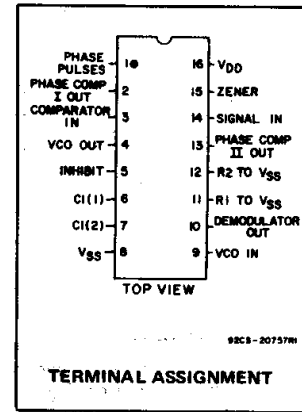
Applications:

■ FM demodulator and modulator
■ Frequency synthesis and multiplication
■ Frequency discriminator
■ Data synchronization
■ Voltage-to-frequency conversion
■ Tone decoding
■ FSK – Modems
■ Signal conditioning
■ (See ICAN-6101) "RCA COS/MOS Phase-Locked Loop – A Versatile Building Block for Micropower Digital and Analog Applications"
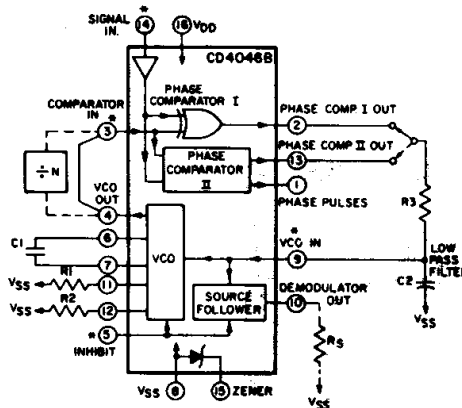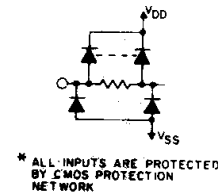

Fig.1 – CMOS phase-locked loop block diagram.

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) .... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS .... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT .... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C .... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) .... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) .... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .... +265°C

Phase Comparators

The phase-comparator signal input (terminal 14) can be direct-coupled provided the signal swing is within CMOS logic levels [logic "0" ≤30% (V_{DD}–V_{SS}), logic "1" ≥ 70% (V_{DD}–V_{SS})]. For smaller swings the signal must be capacitively coupled to the self-biasing amplifier at the signal input.

Phase comparator I is an exclusive-OR network; it operates analogously to an over-driven balanced mixer. To maximize the lock range, the signal- and comparator-input frequencies must have a 50% duty cycle. With no signal or noise on the signal input, this phase comparator has an average output voltage equal to $V_{DD}/2$. The low-pass filter connected to the output of phase comparator
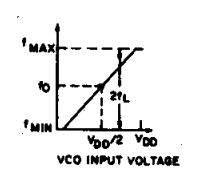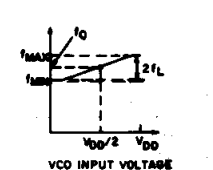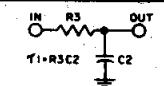
RECOMMENDED OPERATING CONDITIONS at T_A = Full Package-Temperature Range

For maximum reliability, nominal operating conditions should be selected so that
operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	Min.	Max.	
Supply-Voltage Range VCO Section:			
As Fixed Oscillator	3	18	
Phased-Lock-Loop Operation	5	18	V
Supply-Voltage Range Phase Comparator Section:			
Comparators	3	18	
VCO Operation	5	18	

DESIGN INFORMATION

This information is a guide for approximating
the values of external components for the
CD4046B in a Phase-Locked-Loop system.

The selected external components must be
within the following ranges:
$5 \text{ k}\Omega \leqslant$ R1, R2, $R_S \leqslant 1 \text{ M}\Omega$
$C1 \geqslant 100 \text{ pF at } V_{DD} \geqslant 5 \text{ V}$;
$C1 \geqslant 50 \text{ pF at } V_{DD} \geqslant 10 \text{ V}$

Characteristics	Phase Comparator Used	Design Information		
VCO Frequency	1	VCO WITHOUT OFFSET $R_2 = \infty$	VCO WITH OFFSET	
	2	Same as for No.1		
For No.Signal Input	1	VCO will adjust to center frequency, f_o		
	2	VCO will adjust to lowest operating frequency, f_{min}		
Frequency Lock Range, 2 f_L	1	2 f_L = full VCO frequency range		
		2 f_L = $f_{max} - f_{min}$		
	2	Same as for No.1		
Frequency Capture Range, 2 f_C Loop Filter Component Selection	1	(1), (2) $2 f_C \approx \dfrac{1}{\pi}\sqrt{\dfrac{2\pi f_L}{\tau 1}}$ For 2 f_C, see Ref. (2)		
	2	$f_C = f_L$		
Phase Angle Between Signal and Comparator	1	$90°$ at center frequency (f_o) approximating $0°$ and $180°$ at ends of lock range (2 f_L)		
	2	Always $0°$ in lock		
Locks On Harmonic of Center Frequency	1	Yes		
	2	No		
Signal Input Noise Rejection	1	High		
	2	Low		

For further information, see
(1) F. Gardner, "Phase-Lock Techniques" John Wiley and Sons, New York, 1966
(2) G. S. Moschytz, "Miniaturized RC Filters Using Phase-Locked Loop", BSTJ, May, 1965.

I supplies the averaged voltage to the VCO
input, and causes the VCO to oscillate at the
center frequency (f_o).

The frequency range of input signals on
which the PLL will lock if it was initially
out of lock is defined as the frequency cap-
ture range ($2f_c$).

The frequency range of input signals on
which the loop will stay locked if it was
initially in lock is defined as the frequency
lock range ($2f_L$). The capture range is $\leqslant$ the
lock range.

With phase comparator I the range of fre-
quencies over which the PLL can acquire
lock (capture range) is dependent on the
low-pass-filter characteristics, and can be
made as large as the lock range. Phase-com-
parator I enables a PLL system to remain
in lock in spite of high amounts of noise
in the input signal.

One characteristic of this type of phase com-
parator is that it may lock onto input fre-
quencies that are close to harmonics of the
VCO center-frequency. A second charac-
teristic is that the phase angle between the
signal and the comparator input varies be-
tween $0°$ and $180°$, and is $90°$ at the center
frequency. Fig. 2 shows the typical, trian-
gular, phase-to-output response characteristic
of phase-comparator I. Typical waveforms
for a CMOS phase-locked-loop employ-
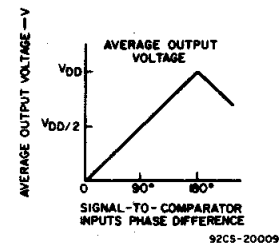ing phase comparator I in locked condition
of f_o is shown in Fig. 3.

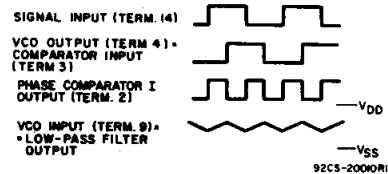*Fig.2 — Phase-comparator I characteristics
at low-pass filter output.*

*Fig. 3—Typical waveforms for CMOS phase-locked
loop employing phase comparator in locked
condition of f_o.*

Phase-comparator II is an edge-controlled
digital memory network. It consists of four
flip-flop stages, control gating, and a three-
state output circuit comprising p- and n-type
drivers having a common output node. When
the p-MOS or n-MOS drivers are ON they
pull the output up to V_{DD} or down to
V_{SS}, respectively. This type of phase com-
parator acts only on the positive edges of
the signal and comparator inputs. The duty
cycles of the signal and comparator inputs
are not important since positive transitions

STATIC ELECTRICAL CHARACTERISTICS

CHARAC-TERISTIC	CONDITIONS VO (V)	VIN (V)	VDD (V)	LIMITS AT INDICATED TEMPERATURES (°C) -55	-40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	UNITS
VCO Section											
Output Low (Sink) Current IOL Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current, IOH Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
Output Voltage: Low-Level, VOL Max.	Term. 4 driving CMOS	0,5	5	0.05				-	0	0.05	
		0,10	10	0.05				-	0	0.05	
		0,15	15	0.05				-	0	0.05	V
Output Voltage: High-Level, VOH Min.	e.g. Term.3	0,5	5	4.95				4.95	5	-	
		0,10	10	9.95				9.95	10	-	
		0,15	15	14.95				14.95	15	-	
Input Current IIN Max.	-	0,18	18	±0.1	±0.1	±1	±1	-	$\pm 10^{-5}$	±0.1	µA
Phase Comparator Section											
Total Device Current, IDD Max. Term. 14 open, Term. 5 = VDD	-	0,5	5	0.2				-	0.1	0.2	
	-	0,10	10	1				-	0.5	1	mA
	-	0,15	15	1.5				-	0.75	1.5	
	-	0,20	20	4				-	2	4	
Term. 14 = VSS or VDD, Term. 5 = VDD	-	0,5	5	20				-	10	20	
	-	0,10	10	40				-	20	40	µA
	-	0,15	15	80				-	40	80	
	-	0,20	20	160				-	80	160	
Output Low (Sink) Current IOL Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	-	
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	-	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	-	
Output High (Source) Current IOH Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	-	mA
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	-	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	-	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	-	
DC-Coupled Signal Input and Comparator Input Voltage Sensitivity Low Level VIL Max.	0.5,4.5	-	5			1.5		-	-	1.5	
	1,9	-	10			3		-	-	3	
	1.5,13.5	-	15			4		-	-	4	V
High Level VIH Min.	0.5,4.5	-	5			3.5		3.5	-	-	
	1,9	-	10			7		7	-	-	
	1.5,13.5	-	15			11		11	-	-	

control the PLL system utilizing this type of comparator. If the signal-input frequency is higher than the comparator-input frequency, the p-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal-input frequency is lower than the comparator-input frequency, the n-type output driver is maintained ON most of the time, and both the n and p drivers OFF (3 state) the remainder of the time. If the signal- and comparator-input frequencies are the same, but the signal input lags the comparator input in phase, the n-type output driver is maintained ON for a time corresponding to the phase difference. If the signal- and comparator-input frequencies are the same, but

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	−55	−40	+85	+125	+25 Min.	+25 Typ.	+25 Max.	
Phase Comparator Section (cont'd)											
Input Current I_{IN} Max. (except Term.14)	—	0,18	18	±0.1	±0.1	±1	±1	—	±10^{−5}	±0.1	µA
3-State Leakage Current, I_{OUT} Max.	0,18	0,18	18	±0.1	±0.1	±0.2	±0.2	—	±10^{-5}	±0.1*	µA

*Limit determined by minimum feasible leakage current measurement for automatic testing.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

CHARACTERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES Min.	LIMITS ALL TYPES Typ.	LIMITS ALL TYPES Max.	UNITS
VCO Section							
Operating Power Dissipation, P_D	f_o = 10 kHz, R_1 = 1 MΩ, $R_2 = \infty$, $VCO_{IN}= \frac{V_{DD}}{2}$		5	—	70	140	µW
			10	—	800	1600	
			15	—	3000	6000	
Maximum Operating Frequency f_{max}	C_1=50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 10 kΩ	5	0.3	0.6	—	MHz
			10	0.6	1.2	—	
			15	0.8	1.6	—	
	C_1 = 50 pF, $R_2 = \infty$, $VCO_{IN}=V_{DD}$	R_1 = 5 kΩ	5	0.5	0.8	—	
			10	1	1.4	—	
			15	1.4	2.4	—	
Center Frequency (f_o) and Frequency Range ($f_{max}-f_{min}$)	Programmable with external components R1, R2, and C1 *See Design Information*						
Linearity	VCO_{IN} = 2.5 V ± 0.3V, R_1=10 kΩ		5	—	1.7	—	%
	=5 V ± 1 V, = 100 kΩ		10	—	0.5	—	
	=5 V ± 2.5 V, =400 kΩ		10	—	4	—	
	=7.5 V ± 1.5 V, = 100 kΩ		15	—	0.5	—	
	= 7.5 V ± 5 V, = 1 MΩ		15	—	7	—	
Temperature – Frequency Stability: No Frequency Offset f_{MIN} = 0			5	—	±0.12	—	%/°C
			10	—	±0.04	—	
			15	—	±0.015	—	
Frequency Offset $f_{MIN} \neq 0$			5	—	±0.09	—	
			10	—	±0.07	—	
			15	—	±0.03	—	
Output Duty Cycle			5,10,15	—	50	—	%
Output Transition Times, t_{THL}, t_{TLH}			5	—	100	200	ns
			10	—	50	100	
			15	—	40	80	

the comparator input lags the signal in phase, the p-type output driver is maintained ON for a time corresponding to the phase difference. Subsequently, the capacitor voltage of the low-pass filter connected to this phase comparator is adjusted until the signal and comparator inputs are equal in both phase and frequency. At this stable point both p- and n-type output drivers remain OFF and thus the phase comparator output becomes an open circuit and holds the voltage on the capacitor of the low-pass filter constant. Moreover the signal at the "phase pulses" output is a high level which can be used for indicating a locked condition. Thus, for phase comparator II, no phase difference exists between signal and comparator input over the full VCO frequency range. Moreover, the power dissipation due to the low-pass filter is reduced when this type of phase comparator is used because both the p- and n-type output drivers are OFF for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range, independent of the low-pass filter. With no signal present at the signal input, the VCO is adjusted to its lowest frequency for phase comparator II. Fig. 10 shows typical waveforms for a CMOS PLL employing phase comparator II in a locked condition.
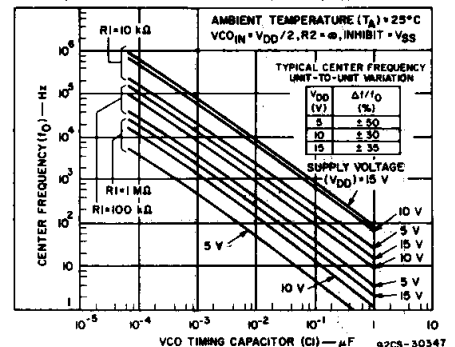
Fig. 4 — Typical center frequency as a function of C1 and R1 at V_{DD} = 5 V, 10 V, and 15 V.
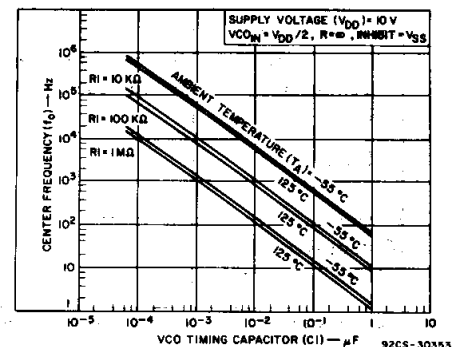

Fig. 5 — Center frequency as a function of C1 and R1 for ambient temperatures of −55°C to 125°C.

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$

CHARAC-TERISTIC	TEST CONDITIONS		V_{DD} (V)	LIMITS ALL TYPES			UNITS
				Min.	Typ.	Max.	
VCO Section (cont'd)							
Source-Follower Output (Demodulated Output): Offset Voltage $\|VCO_{IN} - V_{DEM}\|$	RS > 10 kΩ		5	–	1.8	2.5	V
			10	–	1.8	2.5	
			15	–	1.8	2.5	
Linearity	R_S =100 kΩ = 300 kΩ =500 kΩ	VCO_{IN} = 2.5±0.3 V = 5±2.5 V = 7.5± 5 V	5	–	0.3	–	%
			10	–	0.7	–	
			15	–	0.9	–	
Zener Diode Voltage (V_z)	$I_Z = 50\ \mu A$			4.45	5.5	6.15	V
Zener Dynamic Resistance, R_z	$I_Z = 1\ mA$			–	40	–	Ω
Phase Comparator Section							
Term. 14 (SIGNAL IN) Input Resistance R_{14}			5	1	2	–	MΩ
			10	0.2	0.4	–	
			15	0.1	0.2	–	
AC Coupled Signal Input Voltage Sensitivity* (peak-to-peak)	f_{IN} = 100 kHz, sine wave		5	–	180	360	mV
			10	–	330	660	
			15	–	900	1800	
Propagation Delay Times, Terms. 14 to 1: High to Low Level, t_{PHL}			5	–	225	450	ns
			10	–	100	200	
			15	–	65	130	
Low to High Level, t_{PLH}			5	–	350	700	ns
			10	–	150	300	
			15	–	100	200	
3-State Propagation Delay Times, Terms. 3 to 13: High Level to High Impedance, t_{PHZ}			5	–	225	450	ns
			10	–	100	200	
			15	–	95	190	
Terms. 14 to 13: Low Level to High Impedance, t_{PLZ}			5	–	285	570	ns
			10	–	130	260	
			15	–	95	190	
Input Rise or Fall Times, t_r, t_f Comparator Input, Term. 3	See Fig. 5 for Phase Comp. II output loading		5	–	–	50	μs
			10	–	–	1	
			15	–	–	0.3	
Signal Input, Term. 14			5	–	–	500	μs
			10	–	–	20	
			15	–	–	2.5	
Output Transition Times, t_{THL}, t_{TLH}			5	–	100	200	ns
			10	–	50	100	
			15	–	40	80	

*For sine wave, the frequency must be greater than 10 kHz for Phase Comparator II.
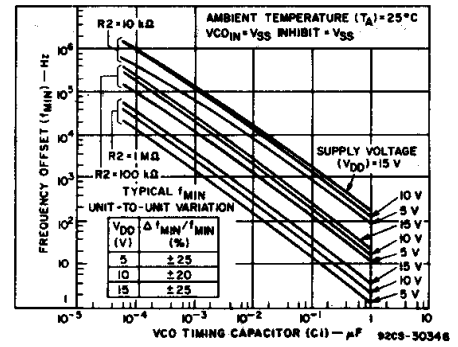
Fig. 6 — Typical frequency offset as a function of C1 and R2 for V_{DD} = 5 V, 10 V, and 15 V.
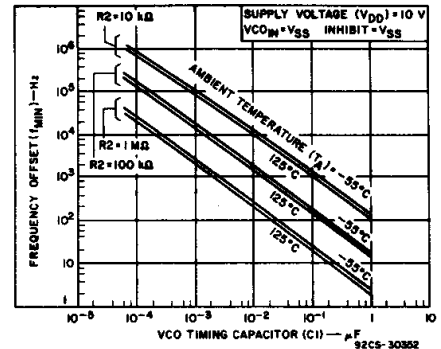
Fig. 7 — Frequency offset as a function of C1 and R2 for ambient temperatures of −55°C to 125°C.
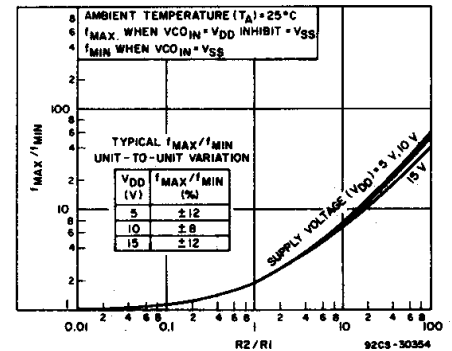
Fig. 8 — Typical f_{MAX}/f_{MIN} as a function of R2/R1.
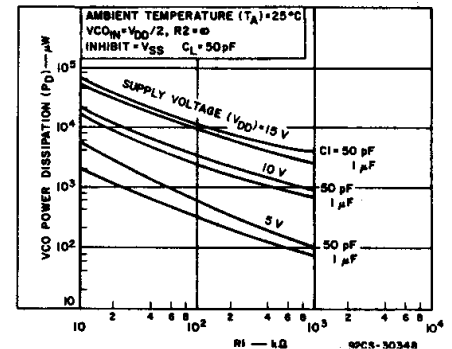
Fig. 9 — Typical VCO power dissipation at center frequency as a function of R1.
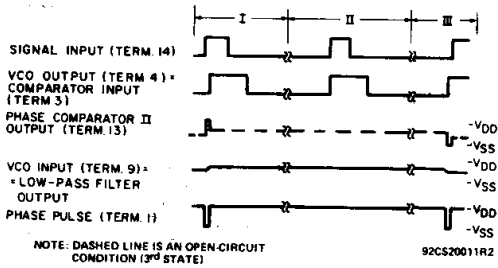
Fig. 10 – Typical waveforms for COS/MOS phase-locked loop employing phase comparator II in locked condition.
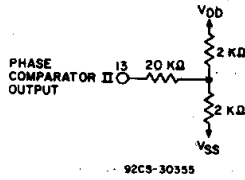
Fig. 11 – Phase comparator II output loading circuit.
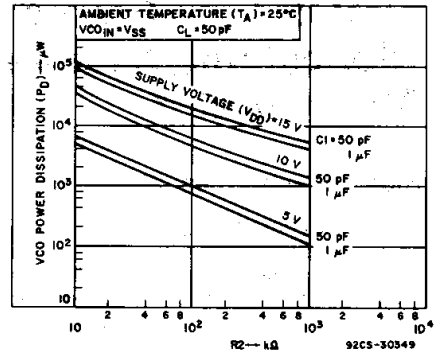
Fig. 12 – Typical VCO power dissipation at f_{MIN} as a function of R2.
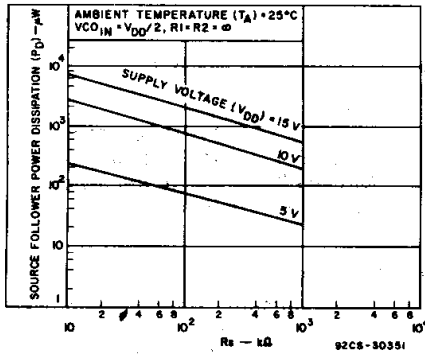
Fig. 13 – Typical source follower power dissipation as a function of Rs.
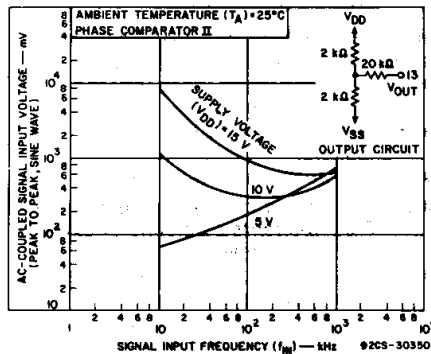
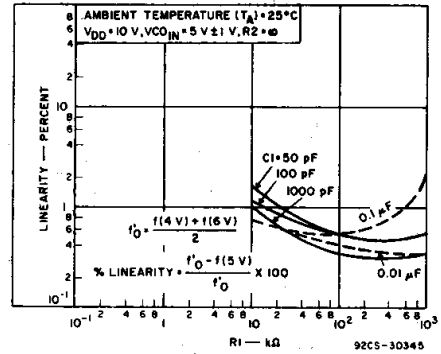Fig. 14 – AC-coupled signal input voltage as a function of signal input frequency.

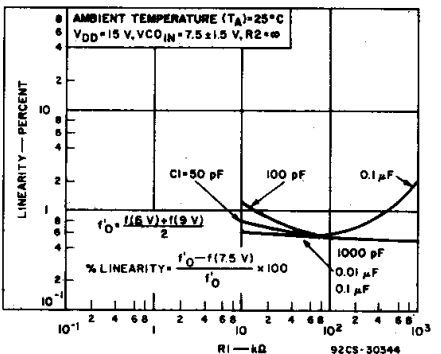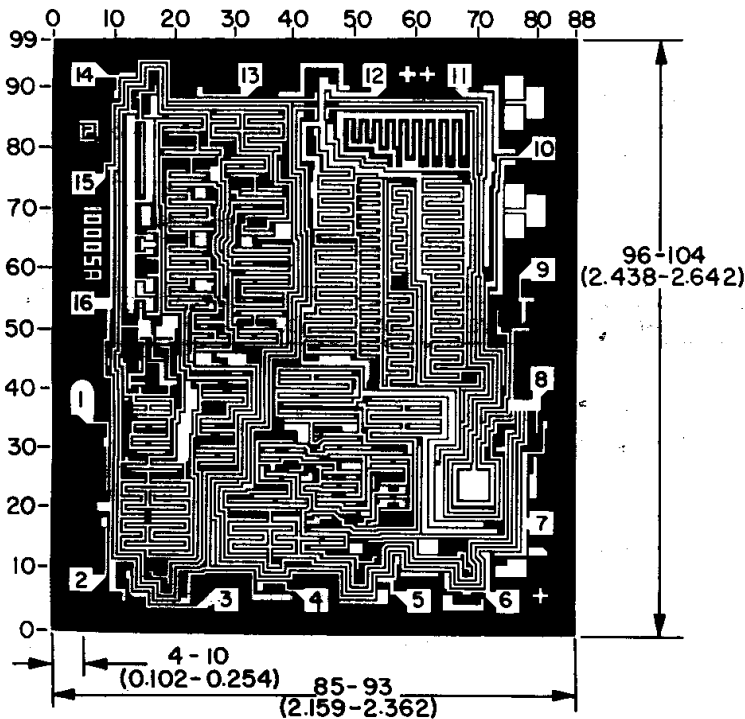Fig. 15 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 10 V.

Fig. 16 – Typical VCO linearity as a function of R1 and C1 at V_{DD} = 15 V.

92CM-36467

Dimensions and pad layout for CD4046BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

3

COMMERCIAL CMOS HIGH VOLTAGE ICs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9466401MEA	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9466401MEA CD4046BF3A	Samples
CD4046BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4046BE	Samples
CD4046BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD4046BE	Samples
CD4046BF	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD4046BF	Samples
CD4046BF3A	ACTIVE	CDIP	J	16	1	TBD	A42	N / A for Pkg Type	-55 to 125	5962-9466401MEA CD4046BF3A	Samples
CD4046BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD4046B	Samples
CD4046BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples
CD4046BPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM046B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4046B, CD4046B-MIL :

• Catalog: CD4046B

• Military: CD4046B-MIL

NOTE: Qualified Version Definitions:

  • Catalog - TI's standard catalog product

  • Military - QML certified for Military and Defense Applications

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4046BNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
CD4046BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD4046BNSR	SO	NS	16	2000	367.0	367.0	38.0
CD4046BPWR	TSSOP	PW	16	2000	367.0	367.0	35.0

NS (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
  B.   This drawing is subject to change without notice.
  C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R—GDIP—T**)   CERAMIC DUAL IN—LINE PACKAGE
14 LEADS SHOWN

DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	——	——	——	——
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

B

14   8

C

1   7

0.065 (1,65)
0.045 (1,14)

0.005 (0,13) MIN

0.060 (1,52)
0.015 (0,38)

0.200 (5,08) MAX

Seating Plane

0.130 (3,30) MIN

0.026 (0,66)
0.014 (0,36)

0.100 (2,54)

A

0°—15°

0.014 (0,36)
0.008 (0,20)

4040083/F 03/03

NOTES: A. All linear dimensions are in inches (millimeters).
         B. This drawing is subject to change without notice.
         C. This package is hermetically sealed with a ceramic lid using glass frit.
         D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
         E. Falls within MIL STD 1835 GDIP1—T14, GDIP1—T16, GDIP1—T18 and GDIP1—T20.

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ 0,10 Ⓜ

16   9

△D△ 4,50   6,60
       4,30   6,20

1   8

5,10
4,90

△C△

0,15 NOM

Gage Plane

0,25

0°−8°

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

◠ 0,10
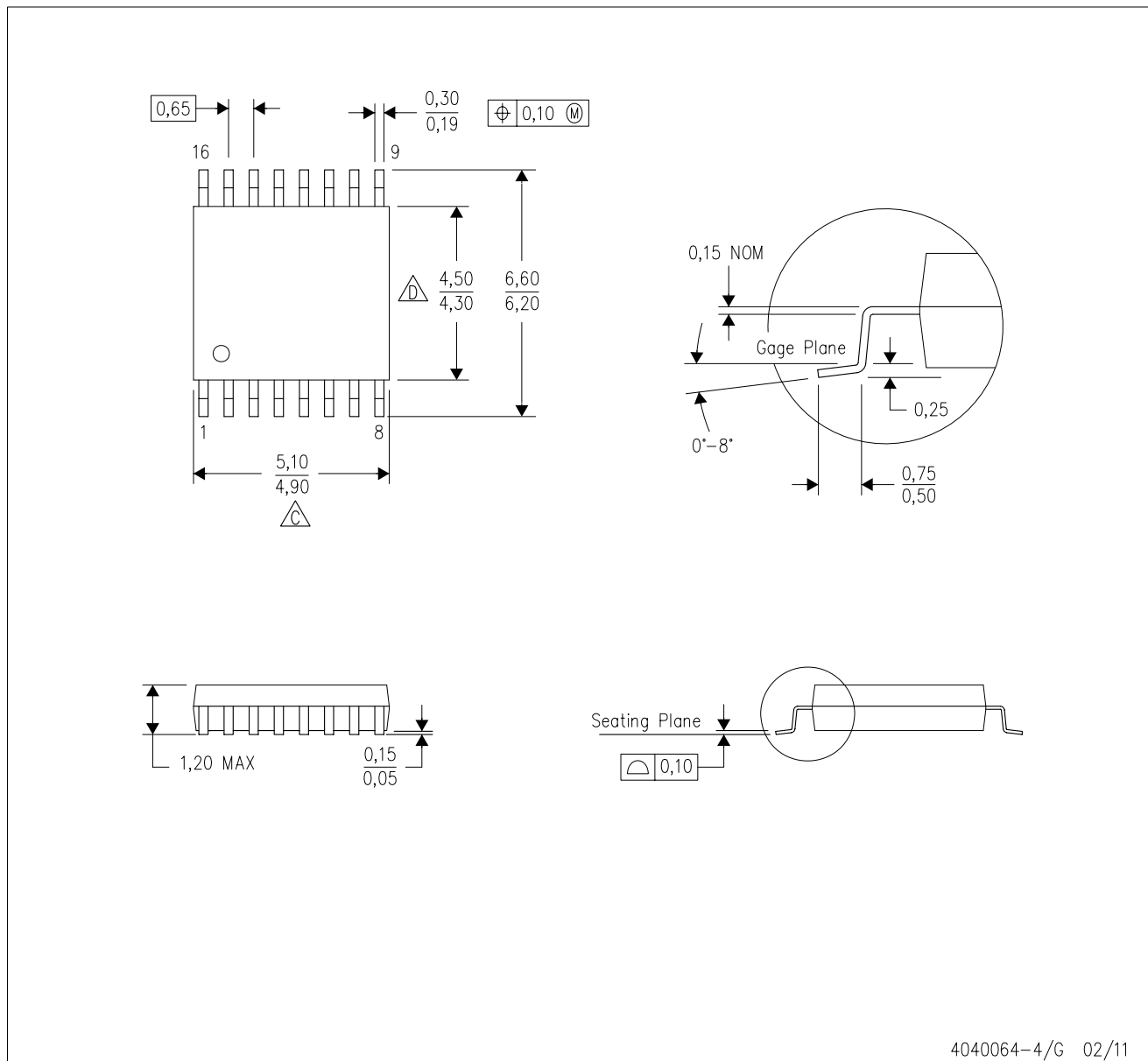
4040064−4/G 02/11

NOTES: A.   All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
         △C△ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
         △D△ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

PW (R−PDSO−G16)   PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

14x0,65

5,60

Stencil Openings
(Note D)

16x0,30

14x0,65

16x1,55

5,60

Example
Non Soldermask Defined Pad

Example
Pad Geometry
(See Note C)

0,35

1,60

0,07

All Around

Example
Solder Mask Opening
(See Note E)
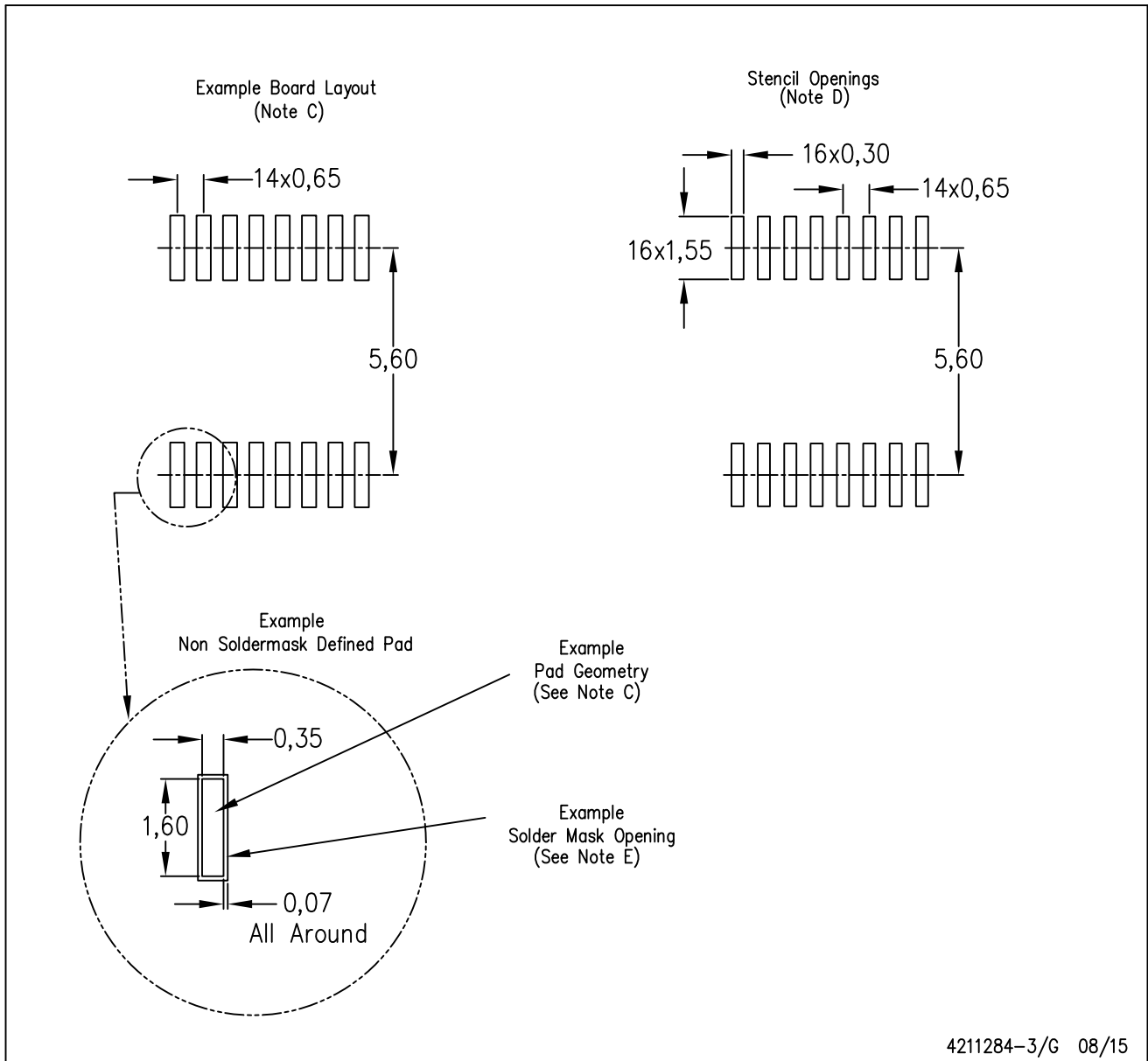
4211284−3/G   08/15

NOTES: A.   All linear dimensions are in millimeters.
          B.   This drawing is subject to change without notice.
          C.   Publication IPC−7351 is recommended for alternate designs.
          D.   Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
               contact their board assembly site for stencil design recommendations. Refer to IPC−7525 for other stencil recommendations.
          E.   Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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N (R−PDIP−T**)   **PLASTIC DUAL−IN−LINE PACKAGE**

16 PINS SHOWN

PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS−001 VARIATION	AA	BB	AC	AD

A

16   9

0.260 (6,60)
0.240 (6,10)

1   8

0.070 (1,78)
0.045 (1,14) △D

△C

0.045 (1,14)
0.030 (0,76) △D

0.020 (0,51) MIN

0.325 (8,26)
0.300 (7,62)

0.015 (0,38)

Gauge Plane

0.200 (5,08) MAX

Seating Plane

0.125 (3,18) MIN

0.010 (0,25) NOM

0.100 (2,54)

0.021 (0,53)
0.015 (0,38)

⊕ 0.010 (0,25) Ⓜ

0.430 (10,92) MAX

14/18 Pin Only
20 Pin vendor option △D

4040049/E 12/2002

NOTES: A. All linear dimensions are in inches (millimeters).
           B. This drawing is subject to change without notice.
        △C Falls within JEDEC MS−001, except 18 and 20 pin minimum body length (Dim A).
        △D The 20 pin end lead shoulder width is a vendor option, either half or full width.

IMPORTANT NOTICE