PAL COLOUR ENCODER AND VIDEO SUMMER

The TEA1002 is mainly intended for video games, add-on teletext applications and colour bar generators for video test equipment. It is a bipolar integrated circuit which converts binary colour information into a PAL composite video output suitable for driving a v.h.f./u.h.f. modulator.

QUICK REFERENCE DATA

Supply voltage (pin 10)	$V_P = V_{10-16}$	nom.	12 V
Supply current at V_P = 12 V	$I_P = I_{10}$	typ.	70 mA
Input voltages (pins, 1, 2, 3, 4, 5, 12, 15, 18)			
LOW	V_{IL}	$\leqslant$	0,8 V
HIGH	V_{IH}	$\geqslant$	2,0 V
Composite video output voltage (pin 8) peak-to-peak value	$V_{8-16(p-p)}$	typ.	3 V
Operating ambient temperature range	T_{amb}		−20 to +65 °C

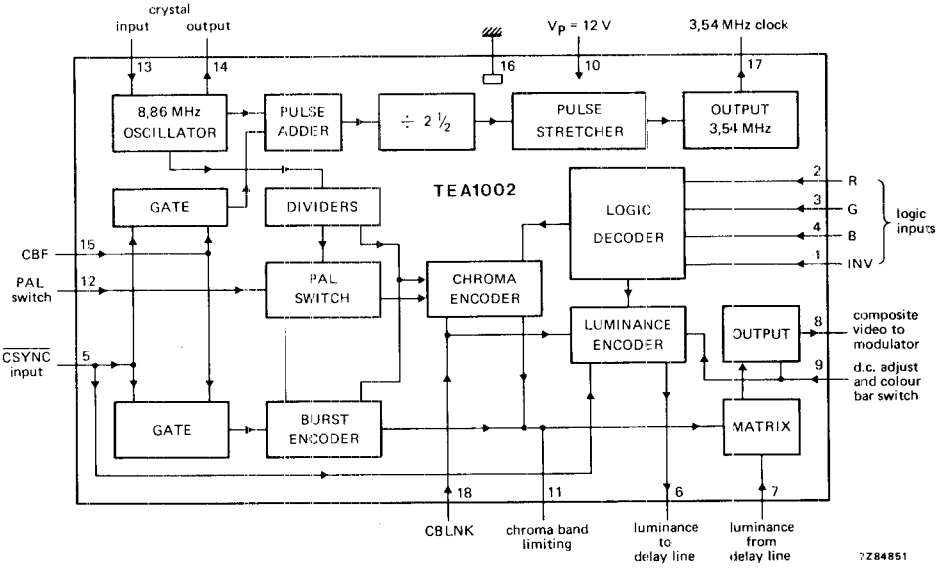


Fig. 1 Block diagram.

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102).

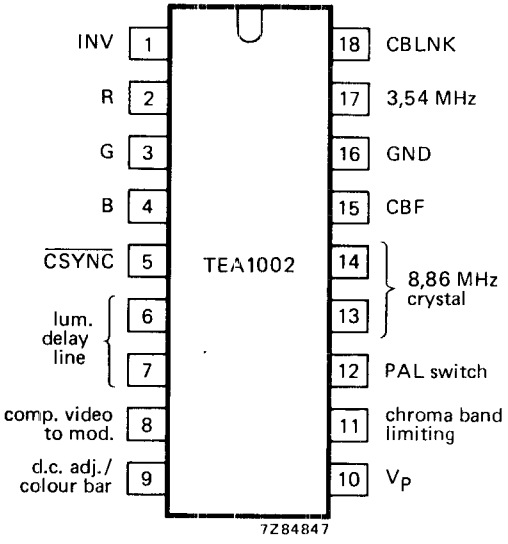


Fig. 2 Pinning diagram.

PINNING

1	INV	inverting logic input
2	R	red logic input
3	G	green logic input
4	B	blue logic input
5	$\overline{\text{CSYNC}}$	composite sync input
6	luminance output to delay line	
7	luminance input from delay line	
8	composite video output to modulator	
9	d.c. adjust and colour bar switch	
10	V_P	supply voltage (+12 V)
11	chroma band limiting	
12	PAL switch input	
13	crystal input	8,86 MHz
14	crystal output	8,86 MHz
15	CBF	colour burst flag input
16	GND	ground
17	3,54 MHz clock output	
18	CBLNK	composite blanking input

GENERAL DESCRIPTION

The TEA1002 PAL colour encoder and video summer IC has an internal 8,86 MHz oscillator from which the 4,43 MHz (R-Y) and B-Y) waveforms are generated. For use in TV games systems, a 3,54 MHz clock output is provided which is buffered via the 2621 sync generator IC. The TEA1002 accepts timing signals (composite sync burst gate, PAL switch and composite blanking) from the 2621 and 4-bit binary coded logic inputs giving colour information from the 2636 programmable video interface IC. The resulting output, which has an adjustable d.c. level, is a 16 colour (including black and white) composite video signal, based on 75% colour bars. Alternatively, with one of the colour inputs connected to ground and the d.c. adjustment disabled, the TEA1002 can be used as a general purpose video encoder providing standard 95% colour bars from RGB logic inputs, suitable for applications such as add-on teletext.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 10)	$V_P = V_{10\text{-}16}$	max. 13,2 V
Input voltage (pins 1, 2, 3, 4, 5, 12, 15, 18) HIGH	V_{IH}	max. V_P V
Storage temperature range	T_{stg}	−25 to +125 °C
Operating ambient temperature range	T_{amb}	−20 to +65 °C

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; measured in Fig. 8; unless otherwise specified

		min.	typ.	max.	
Supply voltage	$V_P = V_{10\text{-}16}$	10,8	12	13,2	V
Supply current	$I_P = I_{10}$	–	70	–	mA
Clock output (pin 17) (notes 1 and 2, Fig. 6)					
Clock cycle time	T	–	282	–	ns
Output voltage (peak-to-peak value) measured into 30 pF load capacitance	$V_{17\text{-}16(p\text{-}p)}$	4	–	6	V
Output rise time into 30 pF load	t_r	–	4	30	ns
Output fall time into 30 pF load	t_f	–	10	30	ns
Clock pulse width LOW measured at + 0,8 V after restoration	t_L	100	140	–	ns
Clock pulse width HIGH measured at + 2,4 V after restoration	t_H	100	130	–	ns
Oscillator stability (pins 13, 14) (notes 3 and 4)					
Variation in internal 4,43 MHz reference clock frequency					
temperature range: −20 to + 25 °C	$\Delta f_{osc}/\Delta T$	–	−0,8	–	Hz/K
+ 25 to + 70 °C	$\Delta f_{osc}/\Delta T$	–	−2,6	–	Hz/K
supply voltage range: 10,8 to 13,2 V	$\Delta f_{osc}/\Delta V_P$	–	−25	–	Hz/V
Timing inputs (pins 5, 12, 15, 18) (Fig. 3)					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2	–	V_P	V
Input current LOW (d.c.); V_I = 0 V	I_{IL}	–	–	100	μA
Input current HIGH (d.c.); V_I = 12 V	I_{IH}	–	–	100	μA
Input capacitance	C_I	–	–	10	pF
Input rise and fall times	t_r, t_f	–	–	200	ns
Colour code inputs (pins 1, 2, 3, 4) (note 6)					
Input voltage LOW	V_{IL}	–	–	0,8	V
Input voltage HIGH	V_{IH}	2	–	V_P	V
Input current LOW (d.c.); V_I = 0 V	I_{IL}	–	–	100	μA
Input current HIGH (d.c.); V_I = 12 V	I_{IH}	–	–	100	μA
Input capacitance	C_I	–	–	10	pF

DEVELOPMENT SAMPLE DATA

CHARACTERISTICS (continued)

		min.	typ.	max.	
Composite video output (pin 8) (note 5, Table 1)					
Output voltage (peak-to-peak value) sync tip to white	$V_{8\text{-}16(p\text{-}p)}$	–	3	–	V
Residual chroma voltage on white (r.m.s. value) (4,43 MHz)	$V_{8\text{-}16(rms)}$	–	30	–	mV
Sync tip d.c. levels					
for $V_{9\text{-}16} = 12$ V	$V_{8\text{-}16}$	–	5,1	–	V
for $V_{9\text{-}16} < 9$ V	$V_{8\text{-}16}$	–	2,6	–	V
D.C. output adjustment (pin 9)					
D.C. adjustment voltage range where $\Delta V_{8\text{-}16} = \Delta V_{9\text{-}16}$	$V_{9\text{-}16}$	9,5	–	12	V
Applied voltages to guarantee					
75% colour bars	$V_{9\text{-}16}$	4	–	–	V
95% colour bars	$V_{9\text{-}16}$	–	–	3	V
Chroma band limiting (pin 11)					
Internal impedance at pin 11	$\lvert Z_i \rvert$	–	1,5	–	kΩ

Notes

1. This circuit assumes capacitive coupling to the N-MOS games IC (see Fig. 5).
2. The integrated circuit gates the CBF and CSYNC signals to provide a 'frame offset' which lengthens two clock periods by 56 ns every field. This provides a subcarrier/line frequency relationship of $f_{sc} = 283¾\ f_l + 25$ Hz which gives an optimum picture response.
3. These figures hold for a typical quartz crystal as specified below:
   Crystal catalogue no. 4322 143 04051, used in series with 20 pF trimmer capacitance (C_L).
   motional resistance (R1): typ. 15 Ω; max. 60 Ω
   static capacitance (C0): typ. 5 pF; max. 6 pF.
4. These figures exclude the temperature dependence of the crystal and load capacitance (C_L).
5. The chroma/luminance phase inequality can be compensated by an external delay line connected between pins 6 and 7 (see Fig. 8).
   For measurements on the composite video output use the circuit as shown in Fig. 7.
6. To generate standard colour bar signals, pin 1 must be grounded externally.

APPLICATION INFORMATION

The function is described against the corresponding pin number

1. **Inverting logic input**

   When this pin is connected to ground, the logic inputs on pins 2, 3 and 4 are decoded as R, G and B respectively and the chrominance signal at the output is at its full amplitude. If this pin is taken HIGH (> 2 V) the logic inputs are decoded as $\overline{R}$, $\overline{G}$ and $\overline{B}$ and the chrominance signal is reduced to half its full amplitude (see Table 1).

2, 3, 4. **Red, green and blue logic inputs**

5. **Composite sync input**

   This pin requires a negative logic composite sync signal ($\overline{CSYNC}$). The signal is also gated with CBF to control a frame offset phase adjustment for the 3,54 MHz clock (see pins 13 and 14).

6, 7. **Luminance delay line**

The combined luminance and sync signal appearing at pin 6 must be d.c. coupled to pin 7 via an appropriate luminance delay line or resistor network. The resistors must have a tolerance of ± 5% (see Fig. 7).

8. **Composite video output**

The output is internally buffered by an emitter follower stage giving a nominal output voltage of 3 V sync-white. The d.c. level is temperature compensated and can be continuously adjusted over a nominally 2,5 V range via an input on pin 9.

9. **D.C. adjustment and colour bar switch**

This pin provides the dual function of d.c. level adjustment for the composite video output stage and colour bar standard selection. An adjustment of $V_{9\text{-}16}$ from 9,5 V to 12 V will cause a corresponding change of output sync tip level from 3 V to 5,5 V (nominal values).

With $V_{9\text{-}16} \geqslant 4$ V the luminance levels are set to give 75% (E.B.U.) colour signals when using the RGB inputs with pin 1 grounded. With $V_{9\text{-}16} \leqslant 3$ V the output levels will be changed to give 95% (B.B.C.) colour signals (see Table 1). Thus d.c. adjustment can only be obtained with 75% colours.

10. **Supply voltage** (+ 12 V)

11. **Chroma band limiting**

This pin is connected internally to the chrominance summing junction and may be used to limit the bandwidth of the chroma signal by connecting it to a 4,43 MHz tuned filter via a blocking capacitor. The internal impedance is nominally 1,5 kΩ. If a filter is used at this point, then the delay of the chroma signals must be compensated by an appropriate luminance delay line between pins 6 and 7.

12. **PAL switch**

This pin requires a logic signal at half line frequency to control the phase of the (R-Y) modulator and the burst signal.

13, 14. **8,86 MHz crystal**

An 8,867238 MHz crystal in series with a trimmer capacitor is connected between these pins to form part of an oscillator. The output of the oscillator is divided to provide the four subcarrier phases required in the encoder.

The 8,86 MHz signal is also divided by 2½ to give a 3,54 MHz clock input to the 2621 sync generator IC. A phase correction is made after every field to ensure the correct subcarrier to line frequency relationship.

15. **Colour burst flag**

This pin requires a positive logic signal to enable the colour burst encoder.

16. **Ground** (0 V)

17. **Clock output**

The 3,54 MHz clock signal from this pin must be a.c. coupled to the 2621 sync generator IC.

18. **Composite blanking**

This pin requires a positive logic composite blanking signal. The colour logic inputs at pins 1 to 4 are gated to logic '0' when this input is HIGH.

APPLICATION INFORMATION (continued)

Table 1. Logic inputs and composite video output

	inputs				colour	nominal outputs			
	pin 2 R	pin 3 G	pin 4 B	pin 1 INV		luminance $V_{9\text{-}16} \geqslant 4$ V (%)	luminance $V_{9\text{-}16} \leqslant 3$ V (%)	chroma phase (degrees)	chroma amplitude (% black-white)
1	0	0	0	0	black	0	0	–	–
2	1	0	0	0	red	22,5	47,5	103	± 48
3	0	1	0	0	green	44	69	241	± 44
4	1	1	0	0	yellow	66,5	91,5	167	± 33
5	0	0	1	0	blue	8,5	33,5	347	± 33
6	1	0	1	0	magenta	31	56	61	± 44
7	0	1	1	0	cyan	52,5	77,5	283	± 48
8	1	1	1	0	white	100	100	–	–
9	0	0	0	1	grey	75	100	–	–
10	1	0	0	1	cyan	52,5	77,5	283	± 24
11	0	1	0	1	magenta	31	56	61	± 22
12	1	1	0	1	blue	8,5	33,5	347	± 17
13	0	0	1	1	yellow	66,5	91,5	167	± 17
14	1	0	1	1	green	44	69	241	± 22
15	0	1	1	1	red	22,5	47,5	103	± 24
16	1	1	1	1	black	0	0	–	–

75% (E.B.U.) colour bars

95% (B.B.C.) colour bars

DEVELOPMENT SAMPLE DATA

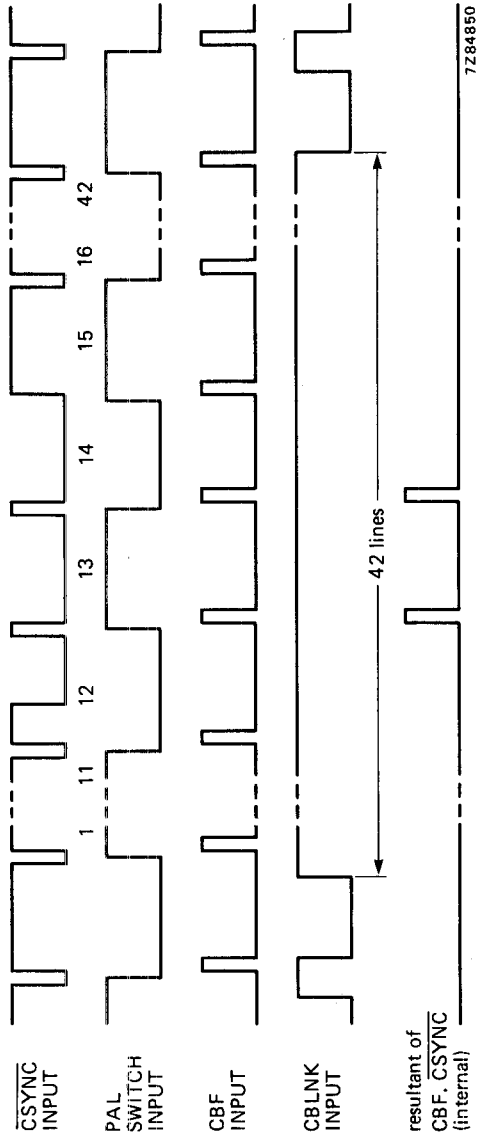


Fig. 3 Timing diagram (signals supplied from sync generator IC).

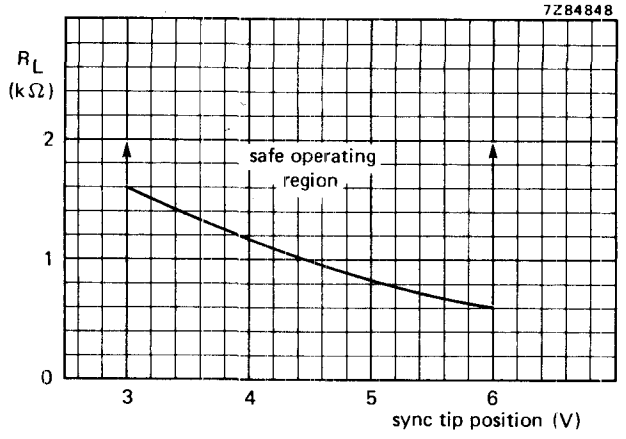


Fig. 4 Safe operating area for load resistor (R_L) at pin 8 as a function of sync tip d.c. position.

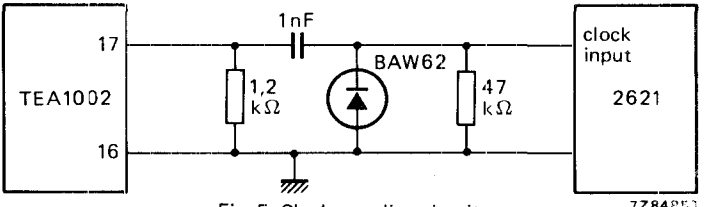


Fig. 5 Clock coupling circuit.

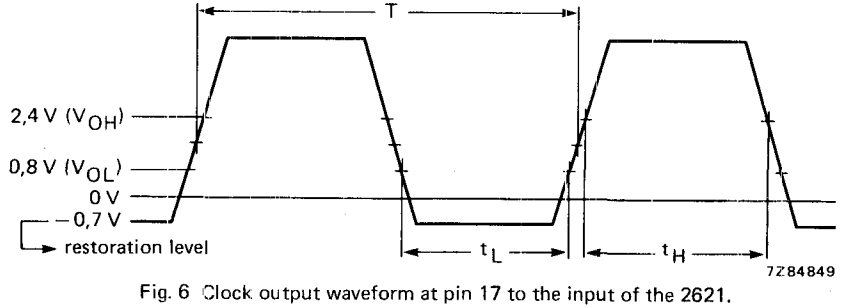


Fig. 6 Clock output waveform at pin 17 to the input of the 2621.

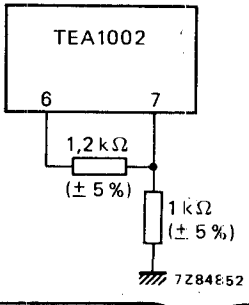
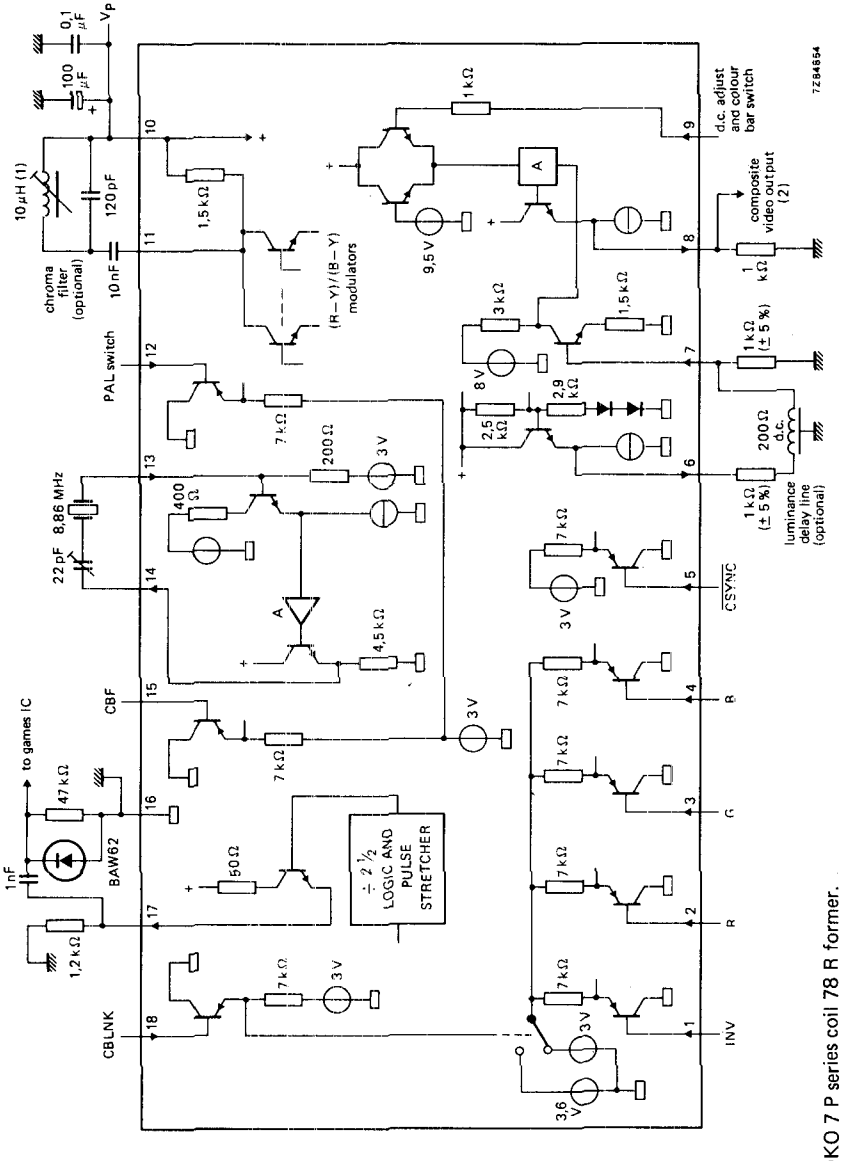


Fig. 7 Connections for pins 6 and 7 when no luminance delay line is used.

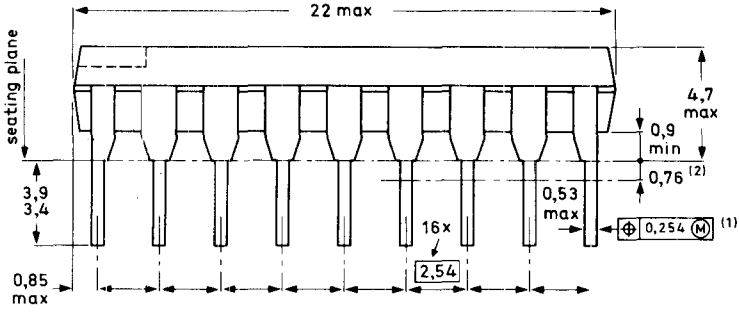
DEVELOPMENT SAMPLE DATA

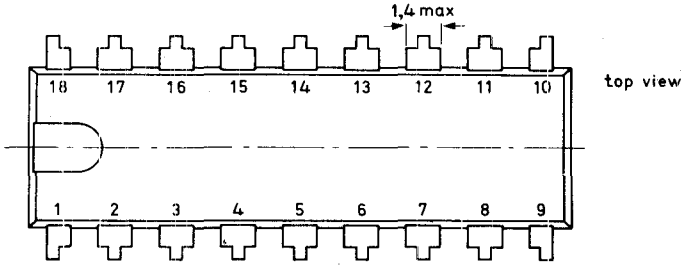


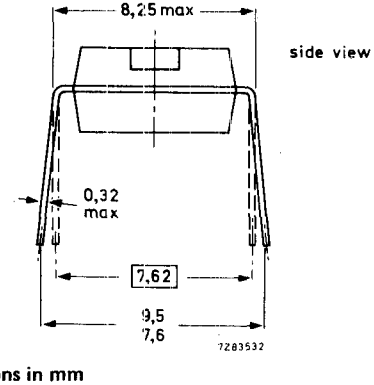
(1) TOKO 7 P series coil 78 R former.
(2) See derating curve Fig. 4.

Fig. 8 Internal circuit details and typical external connections.

18-LEAD DUAL IN-LINE; PLASTIC (SOT-102CS)







⊕ Positional accuracy.

Ⓜ Maximum Material Condition.

(1) Centre-lines of all leads are within ±0,127 mm of the nominal position shown; in the worst case, the spacing between any two leads may deviate from nominal by ±0,254 mm.

(2) Lead spacing tolerances apply from seating plane to the line indicated.

Dimensions in mm

SOLDERING

See next page.

SOLDERING

1. By hand

Apply the soldering iron below the seating plane (or not more than 2 mm above it).
If its temperature is below 300 °C it must not be in contact for more than 10 seconds; if between 300 °C and 400 °C, for not more than 5 seconds.

2. By dip or wave

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.
The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

3. Repairing soldered joints

The same precautions and limits apply as in (1) above.