

MC14513B

BCD-To-Seven Segment Latch/Decoder/Driver

CMOS MSI (Low-Power Complementary MOS)

The MC14513B BCD-to-seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch, an 8421 BCD-to-seven segment decoder, and has output drive capability. Lamp test (\overline{LT}), blanking (\overline{BI}), and latch enable (LE) inputs are used to test the display, to turn-off or pulse modulate the brightness of the display, and to store a BCD code, respectively. The Ripple Blanking Input (RBI) and Ripple Blanking Output (RBO) can be used to suppress either leading or trailing zeroes. It can be used with seven-segment light emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Binary Input
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Capability
- Adds Ripple Blanking In, Ripple Blanking Out to MC14511B
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low-Power TTL Loads, One Low-power Schottky TTL Load to Two HTL Loads Over the Rated Temperature Range.

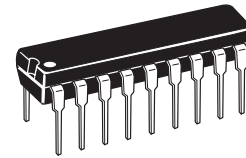
MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (1.)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}	Input Voltage Range, All Inputs	-0.5 to $V_{DD} + 0.5$	V
I	DC Current Drain per Input Pin	10	mA
P_D	Power Dissipation, per Package (2.)	500	mW
T_A	Operating Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
I_{OHmax}	Maximum Continuous Output Drive Current (Source) per Output	25	mA
P_{OHmax}	Maximum Continuous Output Power (Source) per Output (3.)	50	mW



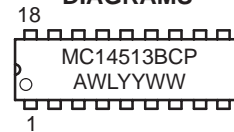
ON Semiconductor

<http://onsemi.com>



MARKING DIAGRAMS

PDIP-18
P SUFFIX
CASE 707



A = Assembly Location
WL or L = Wafer Lot
YY or Y = Year
WW or W = Work Week

ORDERING INFORMATION

Device	Package	Shipping
MC14513BCP	PDIP-18	20/Rail

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

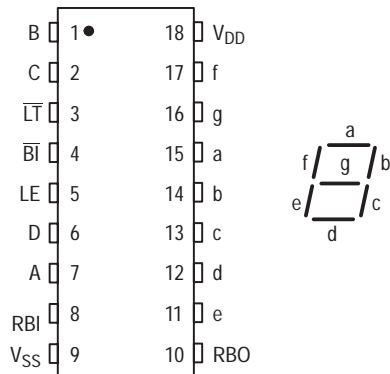
Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

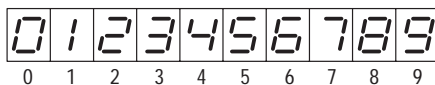
1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating:
Plastic "P and D/DW" Packages: - 7.0 mW/°C
From 65°C To 125°C
3. $P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

MC14513B

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs								Outputs								
RBI	LE	B̄I	L̄T	D	C	B	A	RBO	a	b	c	d	e	f	g	Display
X	X	X	0	X	X	X	X	+	1	1	1	1	1	1	1	8
X	X	0	1	X	X	X	X	+	0	0	0	0	0	0	0	Blank
1	0	1	1	0	0	0	0	1	0	0	0	0	0	0	0	Blank
0	0	1	1	0	0	0	0	0	1	1	1	1	1	1	0	0
X	0	1	1	0	0	0	1	0	0	1	1	0	0	0	0	1
X	0	1	1	0	0	1	0	0	1	1	0	1	1	0	1	2
X	0	1	1	0	0	1	1	0	1	1	1	1	0	0	1	3
X	0	1	1	0	1	0	0	0	0	1	1	0	0	1	1	4
X	0	1	1	0	1	0	1	0	1	0	1	1	0	1	1	5
X	0	1	1	0	1	1	0	0	1	0	1	1	1	1	1	6
X	0	1	1	0	1	1	1	0	1	1	1	0	0	0	0	7
X	0	1	1	1	0	0	0	0	1	1	1	1	1	1	1	8
X	0	1	1	1	0	0	1	0	1	1	1	1	0	1	1	9
X	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
X	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
X	1	1	1	X	X	X	X	†				*				*

X = Don't Care

†RBO = RBI ($\overline{D} \overline{C} \overline{B} \overline{A}$), indicated by other rows of table

*Depends upon the BCD code previously applied when LE = 0

MC14513B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	-55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (4.)	Max	Min	Max		
Output Voltage — Segment Outputs "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.1	—	4.1	5.0	—	4.1		—
			10	9.1	—	9.1	10	—	9.1		—
			15	14.1	—	14.1	15	—	14.1		—
Output Voltage — RBO Output "0" Level $V_{in} = V_{DD}$ or 0	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level $V_{in} = 0$ or V_{DD}	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95		—
			10	9.95	—	9.95	10	—	9.95		—
			15	14.95	—	14.95	15	—	14.95		—
Input Voltage (4.) "0" Level ($V_O = 3.8$ or 0.5 Vdc) ($V_O = 8.8$ or 1.0 Vdc) ($V_O = 13.8$ or 1.5 Vdc)	V_{IL}	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	"1" Level ($V_O = 0.5$ or 3.8 Vdc) ($V_O = 1.0$ or 8.8 Vdc) ($V_O = 1.5$ or 13.8 Vdc)	V_{IH}	5.0	3.5	—	3.5	2.75	—	3.5		—
			10	7.0	—	7.0	5.50	—	7.0		—
			15	11	—	11	8.25	—	11		—
Output Drive Voltage — Segments Source	V_{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc	
			($I_{OH} = 5.0$ mA)	—	—	—	4.24	—	—		—
			($I_{OH} = 10$ mA)	3.9	—	3.9	4.12	—	3.5		—
			($I_{OH} = 15$ mA)	—	—	—	3.94	—	—		—
			($I_{OH} = 20$ mA)	3.4	—	3.4	3.70	—	3.0		—
			($I_{OH} = 25$ mA)	—	—	—	3.54	—	—		—
		10	($I_{OH} = 0$ mA)	9.1	—	9.1	9.58	—	9.1	—	Vdc
			($I_{OH} = 5.0$ mA)	—	—	—	9.26	—	—	—	
			($I_{OH} = 10$ mA)	9.0	—	9.0	9.17	—	8.6	—	
			($I_{OH} = 15$ mA)	—	—	—	9.04	—	—	—	
			($I_{OH} = 20$ mA)	8.6	—	8.6	8.90	—	8.2	—	
			($I_{OH} = 25$ mA)	—	—	—	8.75	—	—	—	
		15	($I_{OH} = 0$ mA)	14.1	—	14.1	14.59	—	14.1	—	Vdc
			($I_{OH} = 5.0$ mA)	—	—	—	14.27	—	—	—	
			($I_{OH} = 10$ mA)	14	—	14	14.18	—	13.6	—	
			($I_{OH} = 15$ mA)	—	—	—	14.07	—	—	—	
			($I_{OH} = 20$ mA)	13.6	—	13.6	13.95	—	13.2	—	
			($I_{OH} = 25$ mA)	—	—	—	13.80	—	—	—	

(continued)

MC14513B

ELECTRICAL CHARACTERISTICS — continued (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
			Min	Max	Min	Typ ^(4.)	Max	Min	Max	
Output Drive Current — RBO Output (V _{OH} = 2.5 V) Source (V _{OH} = 9.5 V) (V _{OH} = 13.5 V) (V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OH}	5.0	-0.40	—	-0.32	-0.64	—	-0.22	—	mAdc
		10	-0.21	—	-0.17	-0.34	—	-0.12	—	
		15	-0.81	—	-0.66	-1.30	—	-0.46	—	
	I _{OL}	5.0	0.18	—	0.15	0.29	—	0.10	—	mAdc
		10	0.47	—	0.38	0.75	—	0.26	—	
		15	1.80	—	1.50	2.90	—	1.0	—	
Output Drive Current — Segments (V _{OL} = 0.4 V) Sink (V _{OL} = 0.5 V) (V _{OL} = 1.5 V)	I _{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
		10	1.6	—	1.3	2.25	—	0.9	—	
		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I _{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Capacitance	C _{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (Per Package) V _{in} = 0 or V _{DD} , I _{out} = 0 μA	I _{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Total Supply Current ^(5.) ^(6.) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0	I _T = (1.9 μA/kHz) f + I _{DD}							μAdc
		10	I _T = (3.8 μA/kHz) f + I _{DD}							
		15	I _T = (5.7 μA/kHz) f + I _{DD}							

4. Noise immunity specified for worst-case input combination.

Noise Margin for both "1" and "0" level =

1.0 Vdc min @ V_{DD} = 5.0 Vdc

2.0 Vdc min @ V_{DD} = 10 Vdc

2.5 Vdc min @ V_{DD} = 15 Vdc

5. The formulas given are for the typical characteristics only at 25°C.

6. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

Input LE and RBI low, and Inputs D, \overline{BI} and \overline{LT} high.

f in respect to a system clock.

All outputs connected to respective C_L loads.

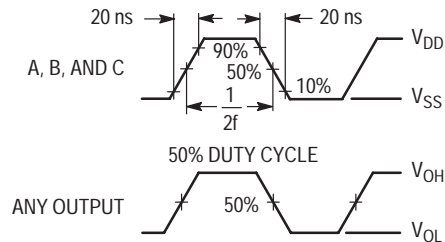


Figure 1. Dynamic Power Dissipation Signal Waveforms

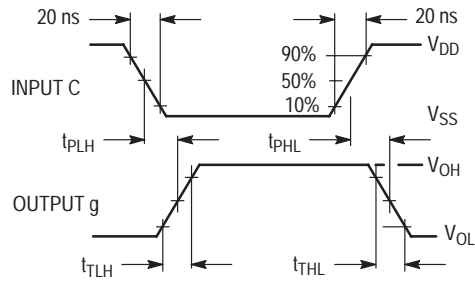
MC14513B

SWITCHING CHARACTERISTICS ^(7.) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

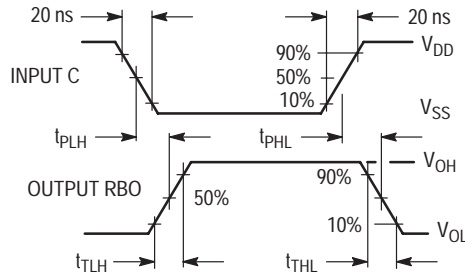
Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time — Segment Outputs	t_{TLH}	5.0 10 15	— — —	40 30 25	80 60 50	ns
Output Rise Time — RBO Output	t_{TLH}	5.0 10 15	— — —	480 240 190	960 480 380	ns
Output Fall Time — Segment Outputs ^(7.) $t_{THL} = (1.5 \text{ ns/pF}) C_L + 50 \text{ ns}$ $t_{THL} = (0.75 \text{ ns/pF}) C_L + 37.5 \text{ ns}$ $t_{THL} = (0.55 \text{ ns/pF}) C_L + 37.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	125 75 65	250 150 130	ns
Output Fall Time — RBO Outputs $t_{THL} = (3.25 \text{ ns/pF}) C_L + 107.5 \text{ ns}$ $t_{THL} = (1.35 \text{ ns/pF}) C_L + 67.5 \text{ ns}$ $t_{THL} = (0.95 \text{ ns/pF}) C_L + 62.5 \text{ ns}$	t_{THL}	5.0 10 15	— — —	270 135 110	540 270 220	ns
Propagation Delay Time — A, B, C, D Inputs ^(7.) $t_{PLH} = (0.40 \text{ ns/pF}) C_L + 620 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 237.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 165 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 655 \text{ ns}$ $t_{PHL} = (0.60 \text{ ns/pF}) C_L + 260 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 182.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	640 250 175	1280 500 350	ns
	t_{PHL}	5.0 10 15	— — —	720 290 200	1440 580 400	ns
Propagation Delay Time — RBI and \overline{BI} Inputs ^(7.) $t_{PLH} = (1.05 \text{ ns/pF}) C_L + 547.5 \text{ ns}$ $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PLH} = (0.30 \text{ ns/pF}) C_L + 135 \text{ ns}$ $t_{PHL} = (0.85 \text{ ns/pF}) C_L + 442.5 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 177.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 142.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	600 200 150	750 300 220	ns
	t_{PHL}	5.0 10 15	— — —	485 200 160	970 400 320	ns
Propagation Delay Time — \overline{LT} Input ^(7.) $t_{PLH} = (0.45 \text{ ns/pF}) C_L + 290.5 \text{ ns}$ $t_{PLH} = (0.25 \text{ ns/pF}) C_L + 112.5 \text{ ns}$ $t_{PLH} = (0.20 \text{ ns/pF}) C_L + 80 \text{ ns}$ $t_{PHL} = (1.3 \text{ ns/pF}) C_L + 248 \text{ ns}$ $t_{PHL} = (0.45 \text{ ns/pF}) C_L + 102.5 \text{ ns}$ $t_{PHL} = (0.35 \text{ ns/pF}) C_L + 72.5 \text{ ns}$	t_{PLH}	5.0 10 15	— — —	313 125 90	625 250 180	ns
	t_{PHL}	5.0 10 15	— — —	313 125 90	625 250 180	ns
Setup Time	t_{su}	5.0 10 15	100 40 30	— — —	— — —	ns
Hold Time	t_h	5.0 10 15	60 40 30	— — —	— — —	ns
Latch Enable Pulse Width	$t_{WL(LE)}$	5.0 10 15	520 220 130	260 110 65	— — —	ns

7. The formulas given are for the typical characteristics only.

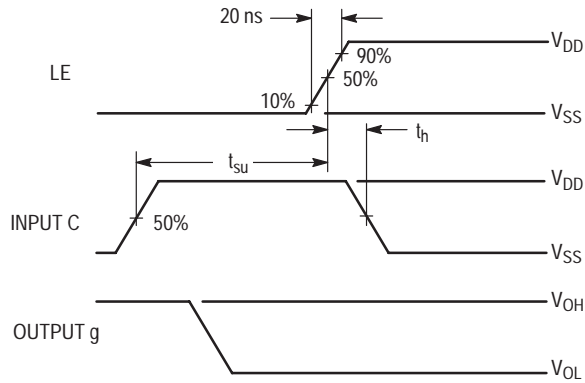
MC14513B



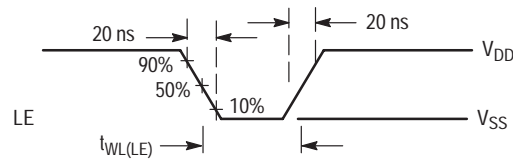
a. Data Propagation Delay: Inputs RBI, D and LE low, and Inputs A, B, \overline{BI} and \overline{LT} high.



b. Inputs A, B, D and LE low, and Inputs RBI, \overline{BI} and \overline{LT} high.



c. Setup and Hold Times: Input RBI and D low, Inputs A, B, \overline{BI} and \overline{LT} high.



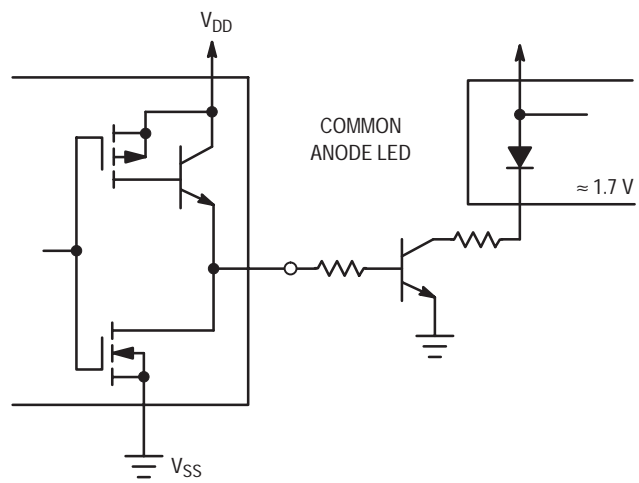
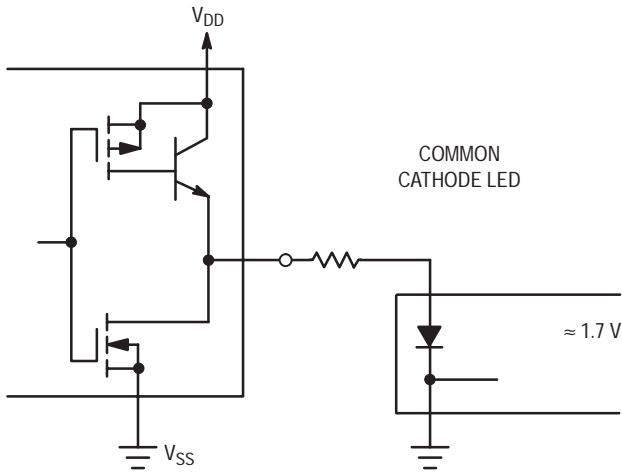
d. Pulse Width: Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

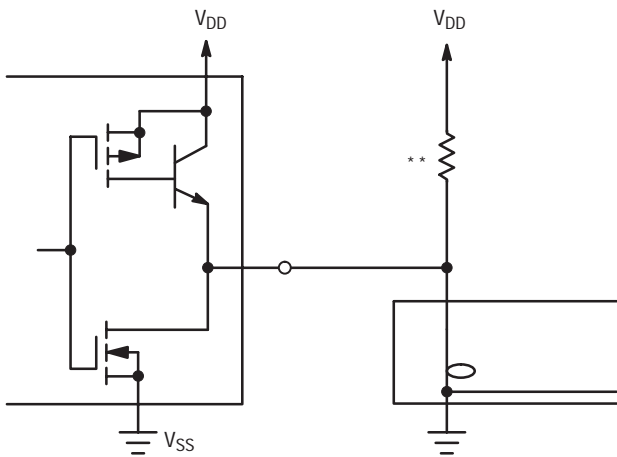
MC14513B

CONNECTIONS TO VARIOUS DISPLAY READOUTS

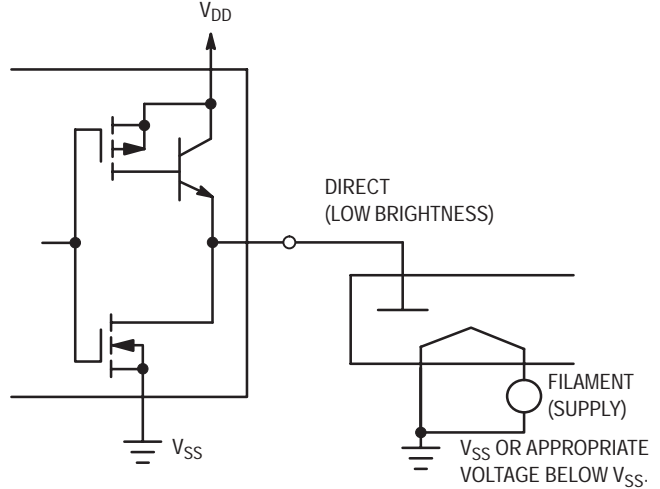
LIGHT EMITTING DIODE (LED) READOUT



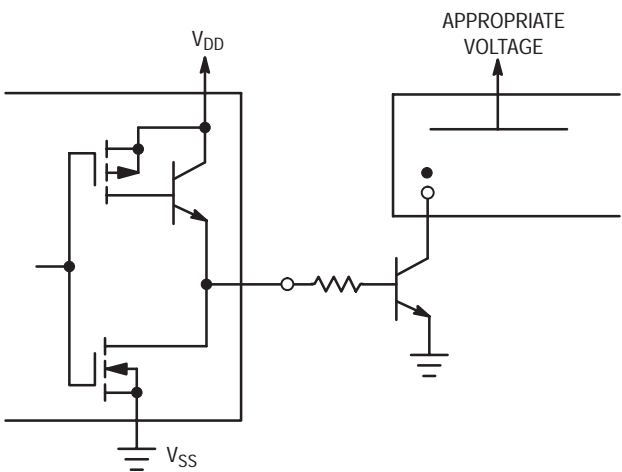
INCANDESCENT READOUT



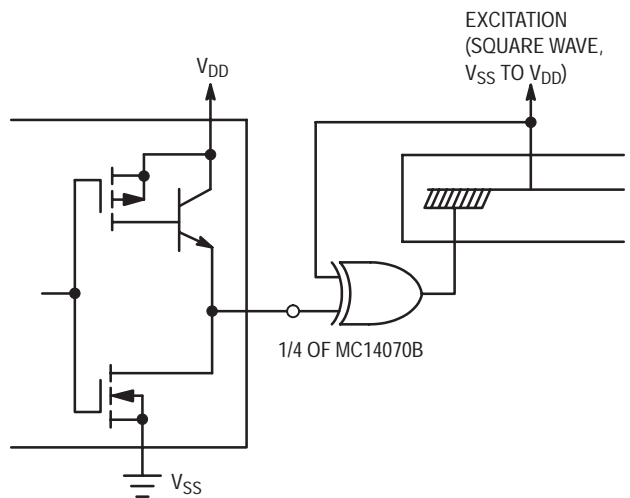
FLUORESCENT READOUT



GAS DISCHARGE READOUT



LIQUID CRYSTAL (LC) READOUT

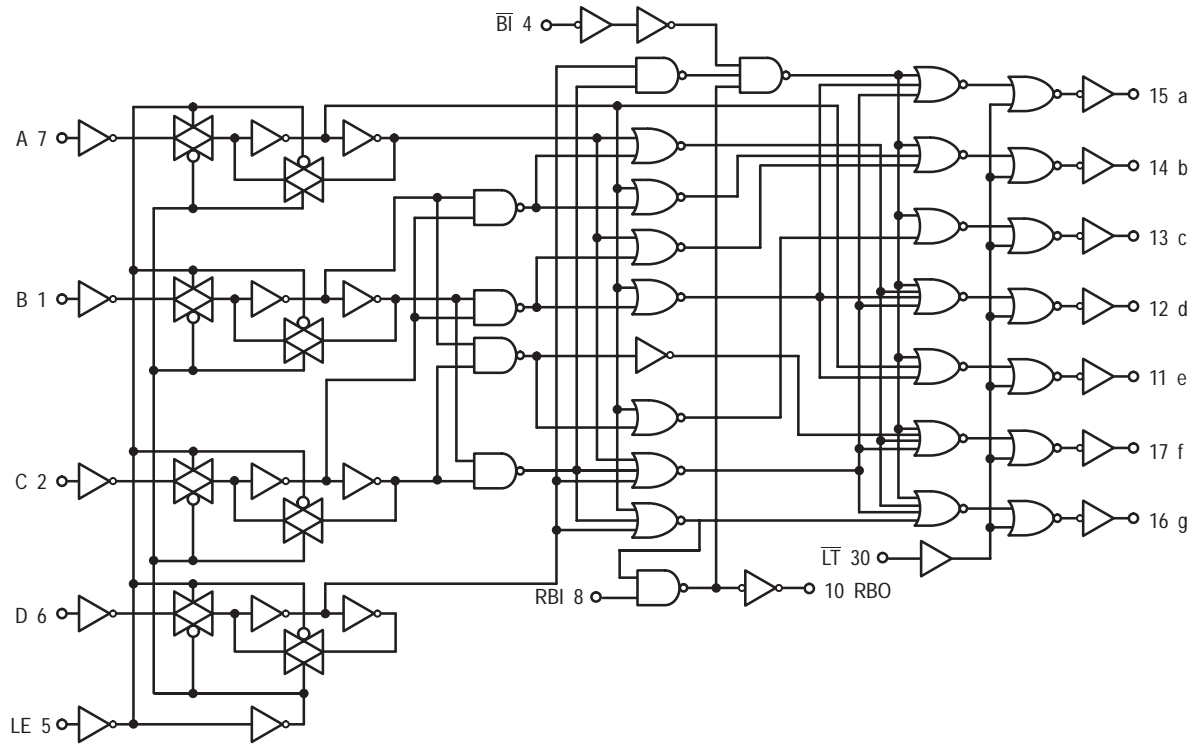


** A filament pre-warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

Direct dc drive of LC's not recommended for life of LC readouts.

MC14513B

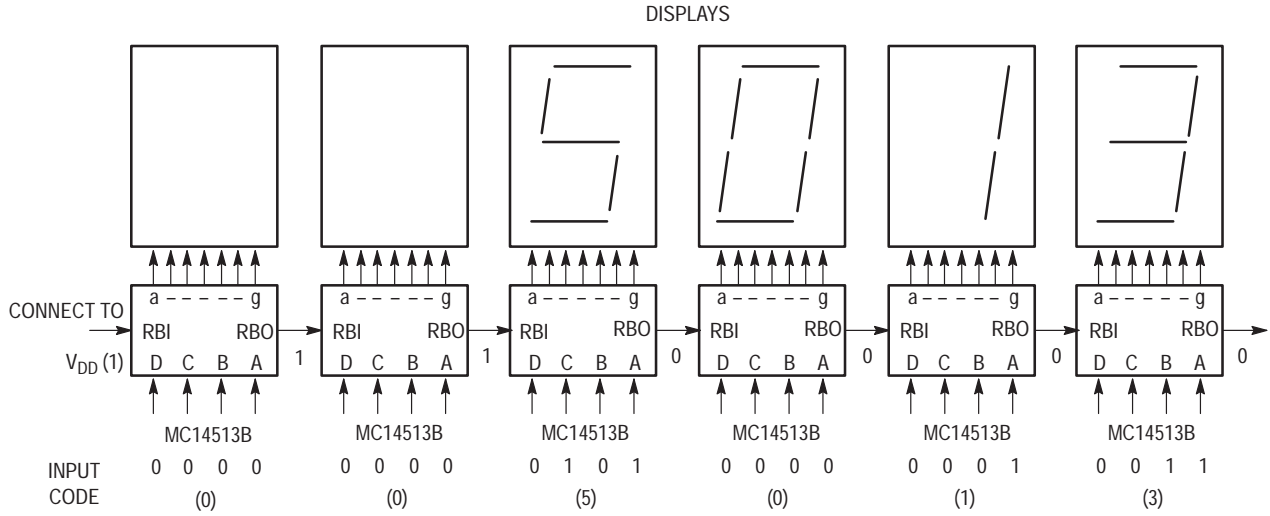
LOGIC DIAGRAM



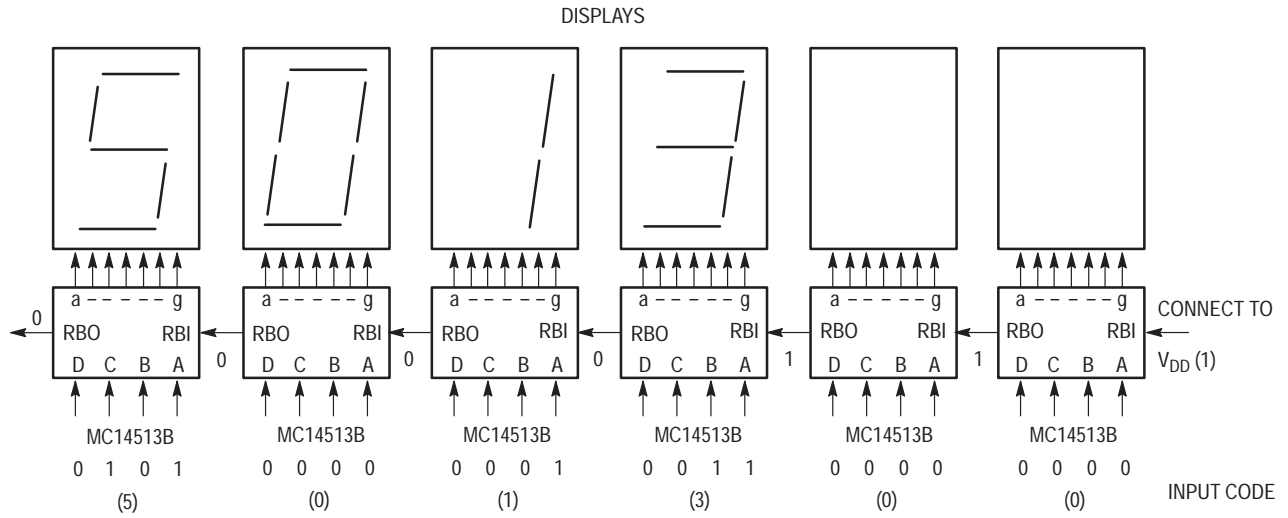
MC14513B

TYPICAL APPLICATIONS FOR RIPPLE BLANKING

LEADING EDGE ZERO SUPPRESSION



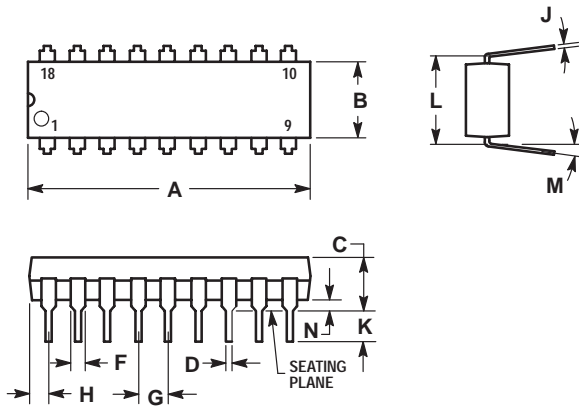
TRAILING EDGE ZERO SUPPRESSION



MC14513B

PACKAGE DIMENSIONS

PDIP-18
P SUFFIX
PLASTIC DIP PACKAGE
CASE 707-02
ISSUE C



NOTES:

1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.875	0.915	22.22	23.24
B	0.240	0.260	6.10	6.60
C	0.140	0.180	3.56	4.57
D	0.014	0.022	0.36	0.56
F	0.050	0.070	1.27	1.78
G	0.100 BSC		2.54 BSC	
H	0.040	0.060	1.02	1.52
J	0.008	0.012	0.20	0.30
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0° 15°		0° 15°	
N	0.020	0.040	0.51	1.02

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

NORTH AMERICA Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com
Fax Response Line: 303-675-2167 or 800-344-3810 Toll Free USA/Canada

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 1:00pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 1:00pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 12:00pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

EUROPEAN TOLL-FREE ACCESS*: 00-800-4422-3781

*Available from Germany, France, Italy, England, Ireland

CENTRAL/SOUTH AMERICA:

Spanish Phone: 303-308-7143 (Mon-Fri 8:00am to 5:00pm MST)
Email: ONlit-spanish@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong & Singapore:
001-800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local Sales Representative.