LF411-N Low Offset, Low Drift JFET Input Operational Amplifier

1 Features

- Internally Trimmed Offset Voltage: 0.5 mV (Max)
- Input Offset Voltage Drift: 7 µV/°C (Typ)
- Low Input Bias Current: 50 pA
- Low Input Noise Current: 0.01 pA/√Hz
- Wide Gain Bandwidth: 3 MHz (Min)
- High Slew Rate: 10 V/µs (Min)
- Low Supply Current: 1.8 mA
- High Input Impedance: $10^{12}\Omega$
- Low Total Harmonic Distortion: ≤0.02%
- Low $1/f$ Noise Corner: 50 Hz
- Fast Settling Time to 0.01%: 2 µs

2 Applications

- High Speed Integrators
- Fast D/A Converters
- Sample and Hold Circuits

3 Description

These devices are low-cost, high-speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

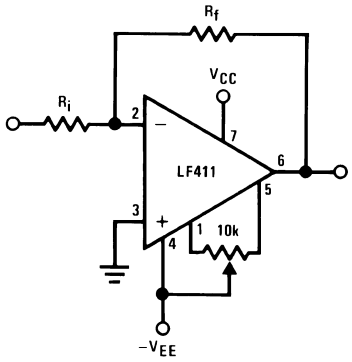
These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LF411-N	8-Pin PDIP	9.59mm×6.35mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Inverting Amplifier with V_{OS} Adjust



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (March 2013) to Revision E — **Page**

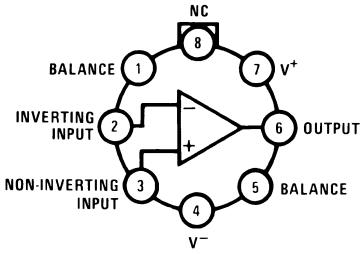
- Added *Handling Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Input Offset Voltage Drift Feature from Max to Typ. ... 1
- Deleted the word "specified" in first sentence of Description paragraph. ... 1
- Deleted note. ... 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LM411A. ... 5
- Deleted $\Delta V_{OS}/\Delta T$ Max specification for LM411. ... 5

Changes from Revision C (March 2013) to Revision D — **Page**

- Changed layout of National Data Sheet to TI format ... 12

5 Pin Configuration and Functions

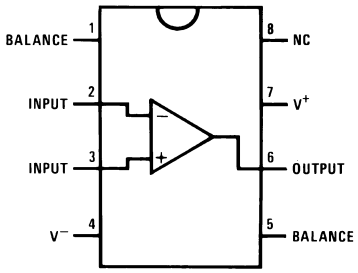
TO
8-Pin
Top View



NOTE: See Package Number NEV0008A

NOTE: Pin 4 connected to case.

PDIP
8-Pin
Top View



NOTE: See Package Number P0008E

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
Balance	1	I	V_{OS} Balance
Inverting Input	2	I	Inverting INput
Non-Inverting Input	3	I	Non-Inverting Input
V-	4	P	Negative Supply
Balance	5	I	V_{OS} Balance
Output	6	O	Output
V+	7	P	Positive Supply
NC	8	NC	No Connect

6 Specifications

6.1 Absolute Maximum Ratings(1)

	LF411A		LF411		UNIT
	MIN	MAX	MIN	MAX	
Supply Voltage		±22		±18	V
Differential Input Voltage		±38		±30	V
Input Voltage Range(2)		±19		±15	V
Output Short Circuit Duration		Continuous		Continuous	

	TO Package		PDIP Package		UNIT
	MIN	MAX	MIN	MAX	
Power Dissipation(3) (4)		670		670	mW
$T_j$max		150		115	°C
Operating Temperature		See (5)		See (5)	
Lead Temperature (Soldering, 10 s)		260		260	°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
(3) For operating at elevated temperature, these devices must be derated based on a thermal resistance of θ_jA.
(4) Max. Power Dissipation is defined by the package characteristics. Operating the part near the Max. Power Dissipation may cause the part to operate outside specified limits.
(5) These devices are available in both the commercial temperature range $0°C \le T_A \le 70°C$ and the military temperature range $-55°C \le T_A \le 125°C$. The temperature range is designated by the position just before the package type in the device number. A "C" indicates the commercial temperature range and an "M" indicates the military temperature range. The military temperature range is available in the TO package only.

6.2 Handling Ratings

		MIN	MAX	UNIT
T_{stg}	Storage temperature range	−65	150	°C

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply Voltage LF411A			±20	V
Supply Voltage LF411			±15	V

6.4 Thermal Information

THERMAL METRIC(1)			TO	PDIP	UNIT
			8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Still Air	162		°C/W
		400 LF/min Air Flow	65		
$R_{\theta JA}$	Junction-to-ambient thermal resistance			120	
$R_{\theta JC}$	Junction-to-case (top) thermal resistance		20		

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 DC Electrical Characteristics (1)(2)

PARAMETER		TEST CONDITIONS		LF411A			LF411			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	R_S=10 kΩ, T_A=25°C			0.3	0.5		0.8	2.0	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	R_S=10 kΩ			7			7		µV/°C
I_{OS}	Input Offset Current	V_S=±15V (2) (3)	T_j=25°C		25	100		25	100	pA
			T_j=70°C			2			2	nA
			T_j=125°C			25			25	nA
I_B	Input Bias Current	V_S=±15V (2) (3)	T_j=25°C		50	200		50	200	pA
			T_j=70°C			4			4	nA
			T_j=125°C			50			50	nA
R_{IN}	Input Resistance	T_j=25°C			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	V_S=±15V, V_O=±10V, R_L=2k, T_A=25°C		50	200		25	200		V/mV
		Over Temperature		25	200		15	200		V/mV
V_O	Output Voltage Swing	V_S=±15V, R_L=10k		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common-Mode Voltage Range			±16	+19.5		±11	+14.5		V
					−16.5			−11.5		V
CMRR	Common-Mode Rejection Ratio	R_S≤10k		80	100		70	100		dB
PSRR	Supply Voltage Rejection Ratio	See (4)		80	100		70	100		dB
I_S	Supply Current				1.8	2.8		1.8	3.4	mA

(1) RETS 411X for LF411MH and LF411MJ military specifications.
(2) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF411A and for V_S=±15V for the LF411. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.
(3) The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j=T_A+\theta_{jA} P_D$ where θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
(4) Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice, from ±15V to ±5V for the LF411 and from ±20V to ±5V for the LF411A.

6.6 AC Electrical Characteristics

PARAMETER (1)(2)		TEST CONDITIONS	LF411A			LF411			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S=±15V, T_A=25°C	10	15		8	15		V/µs
GBW	Gain-Bandwidth Product	V_S=±15V, T_A=25°C	3	4		2.7	4		MHz
e_n	Equivalent Input Noise Voltage	T_A=25°C, R_S=100Ω, f=1 kHz		25			25		nV / √Hz
i_n	Equivalent Input Noise Current	T_A=25°C, f=1 kHz		0.01			0.01		pA / √Hz
THD	Total Harmonic Distortion	A_V=+10, R_L=10k, V_O=20 Vp-p, BW=20 Hz−20 kHz		<0.02 %			<0.02 %		

(1) Unless otherwise specified, the specifications apply over the full temperature range and for V_S=±20V for the LF411A and for V_S=±15V for the LF411. V_{OS}, I_B, and I_{OS} are measured at V_{CM}=0.
(2) RETS 411X for LF411MH and LF411MJ military specifications.

6.7 Typical Performance Characteristics

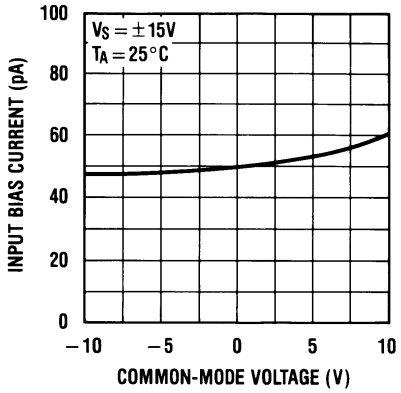


Figure 1. Input Bias Current

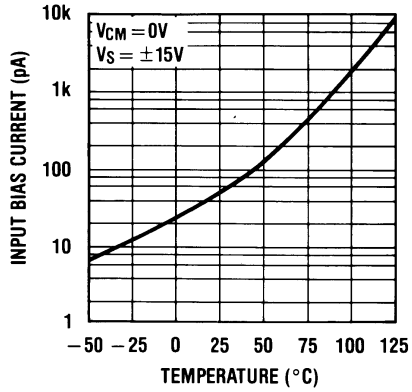


Figure 2. Input Bias Current

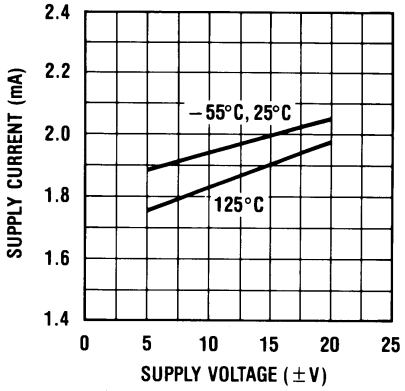


Figure 3. Supply Current

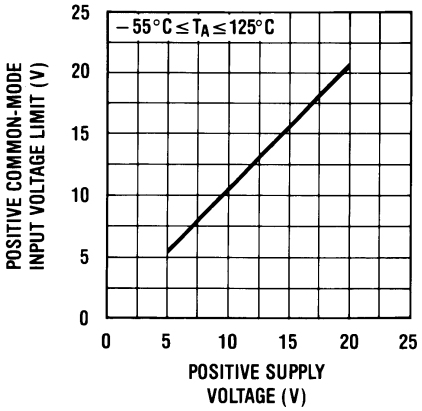


Figure 4. Positive Common-Mode Input Voltage Limit

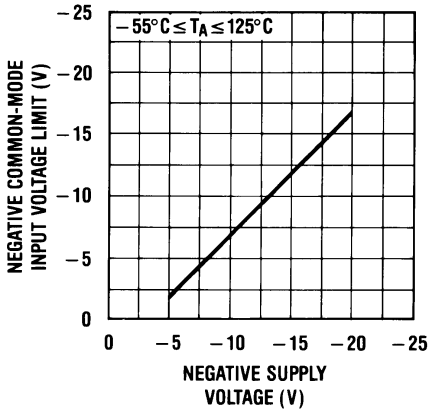


Figure 5. Negative Common-Mode Input Voltage Limit

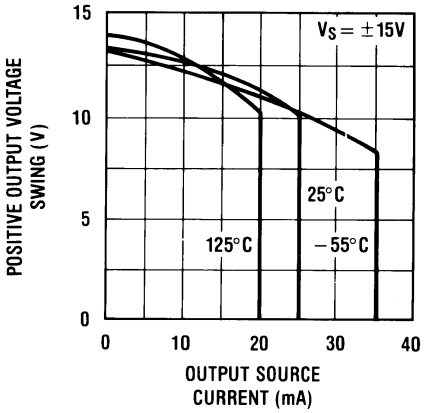


Figure 6. Positive Current Limit

Typical Performance Characteristics (continued)

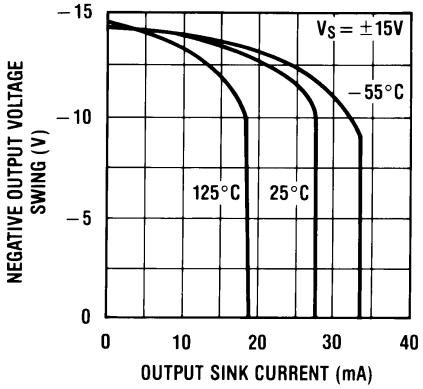


Figure 7. Negative Current Limit

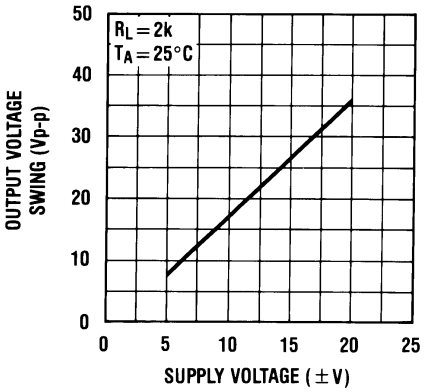


Figure 8. Output Voltage Swing

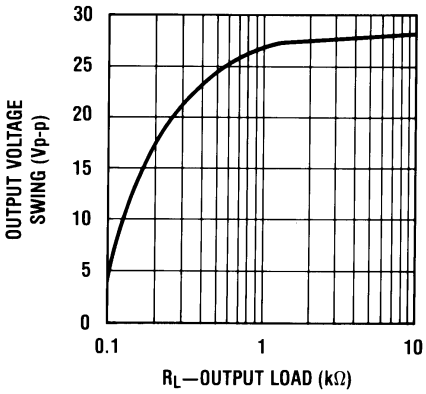


Figure 9. Output Voltage Swing

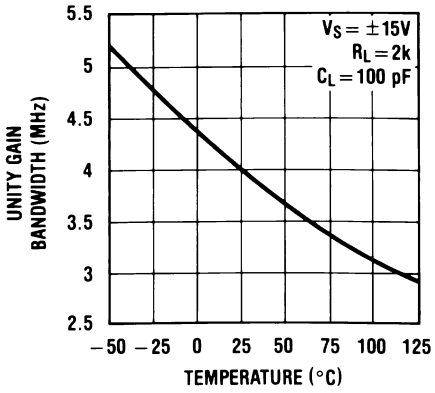


Figure 10. Gain Bandwidth

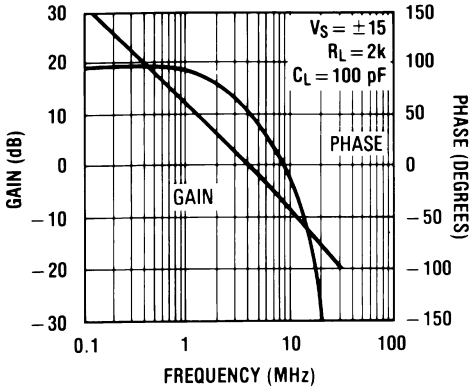


Figure 11. Bode Plot

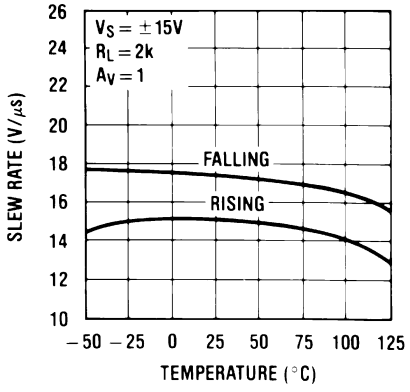


Figure 12. Slew Rate

Typical Performance Characteristics (continued)

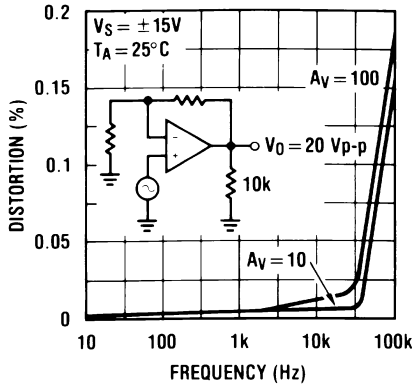


Figure 13. Distortion vs Frequency

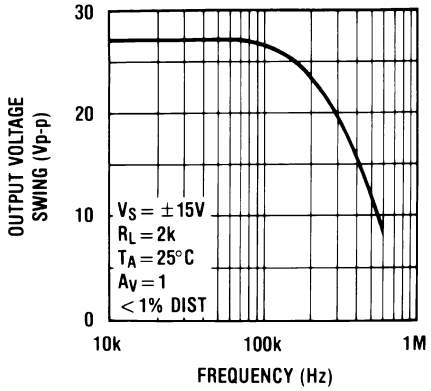


Figure 14. Undistorted Output Voltage Swing

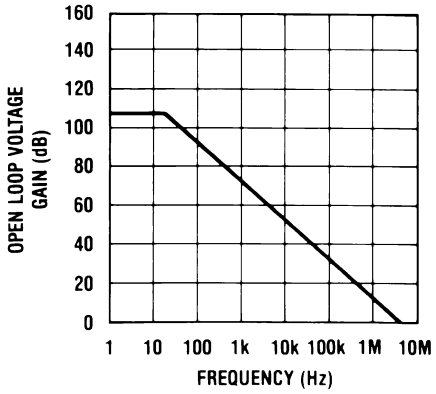


Figure 15. Open Loop Frequency Response

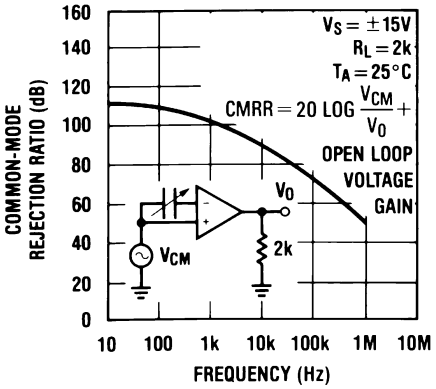


Figure 16. Common-Mode Rejection Ratio

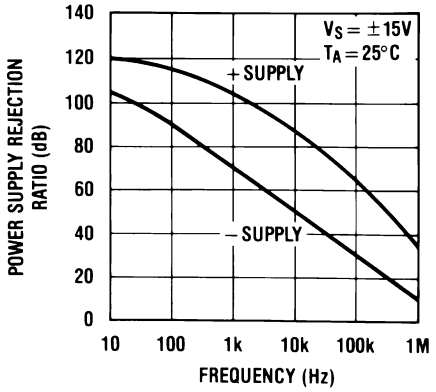


Figure 17. Power Supply Rejection Ratio

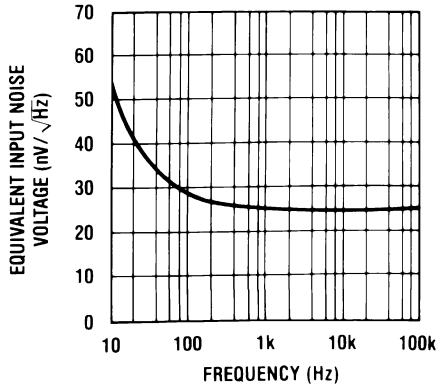


Figure 18. Equivalent Input Noise Voltage

Typical Performance Characteristics (continued)

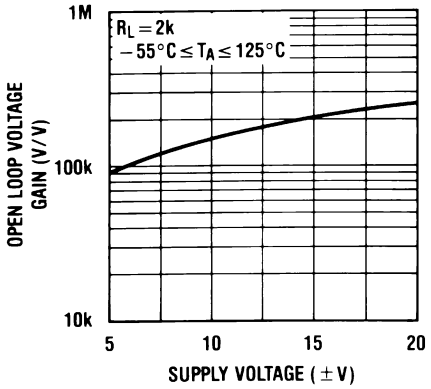


Figure 19. Open Loop Voltage Gain

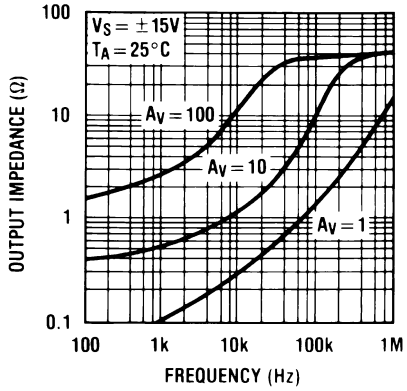


Figure 20. Output Impedance

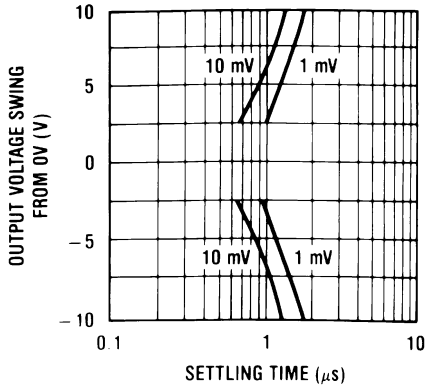


Figure 21. Inverter Settling Time

6.8 Pulse Response (R_L=2 kΩ, C_L=10 pF)

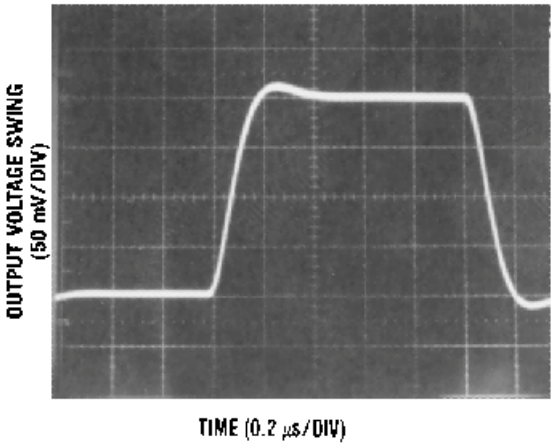


Figure 22. Small Signal Inverting

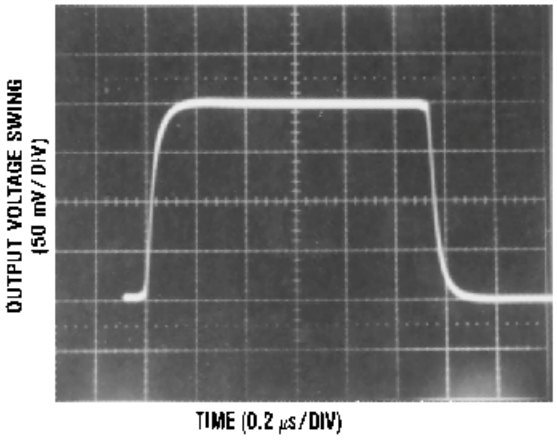


Figure 23. Small Signal Non-Inverting

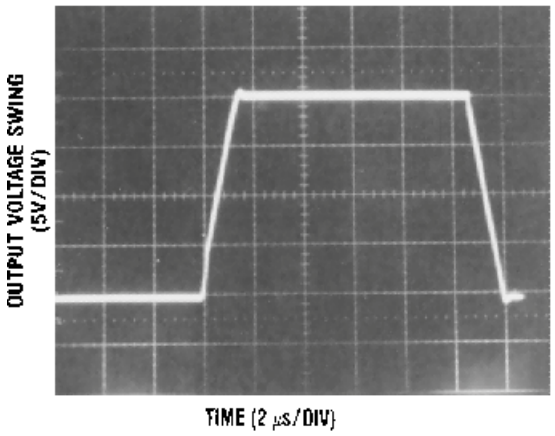


Figure 24. Large Signal Inverting

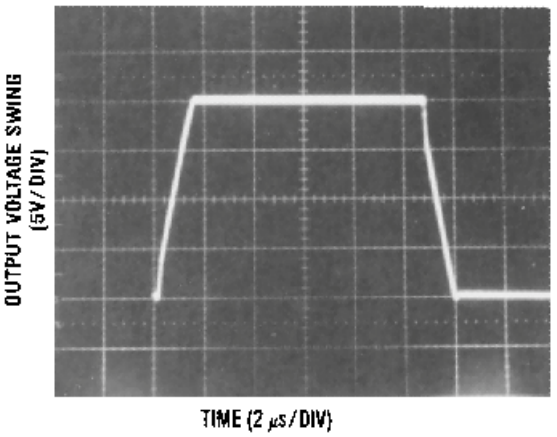


Figure 25. Large Signal Non-Inverting

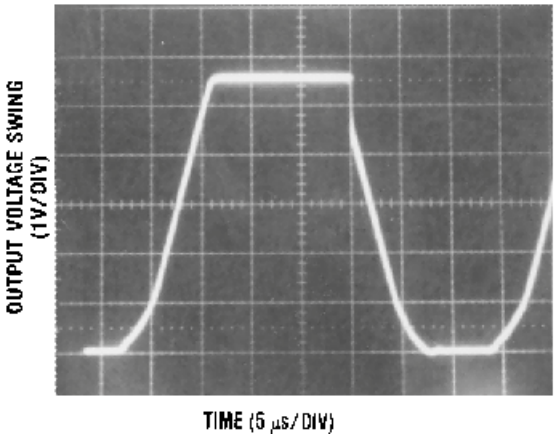


Figure 26. Current Limit (R_L= 100 Ω)

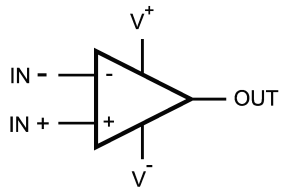
7 Detailed Description

7.1 Overview

These devices are low-cost, high-speed, JFET input operational amplifiers with very low input offset voltage and input offset voltage drift. They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The LF411 is pin compatible with the standard LM741 allowing designers to immediately upgrade the overall performance of existing designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage and drift, low input bias current, high input impedance, high slew rate and wide bandwidth.

7.2 Functional Block Diagram



7.3 Feature Description

The amplifier's differential inputs consist of a non-inverting input (+IN) and an inverting input (-IN). The amplifier amplifies only the difference in voltage between the two inputs, which is called the differential input voltage. The output voltage of the op-amp V_{OUT} is given by the equation $V_{OUT} = A_{OL}(IN+ - IN-)$.

7.4 Device Functional Modes

7.4.1 Simplified Schematic

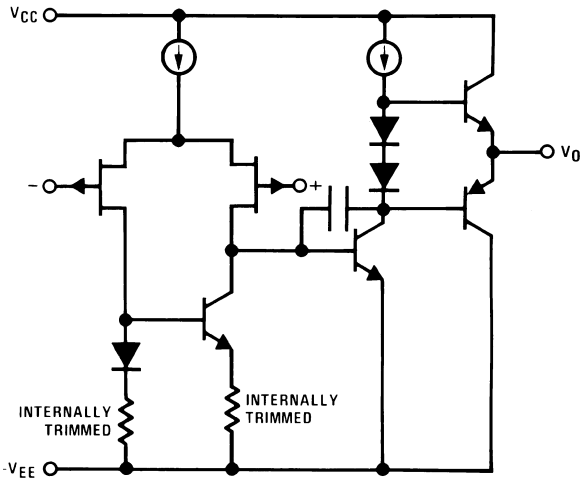


Figure 27. Simplified Schematic

Device Functional Modes (continued)

7.4.2 Detailed Schematic

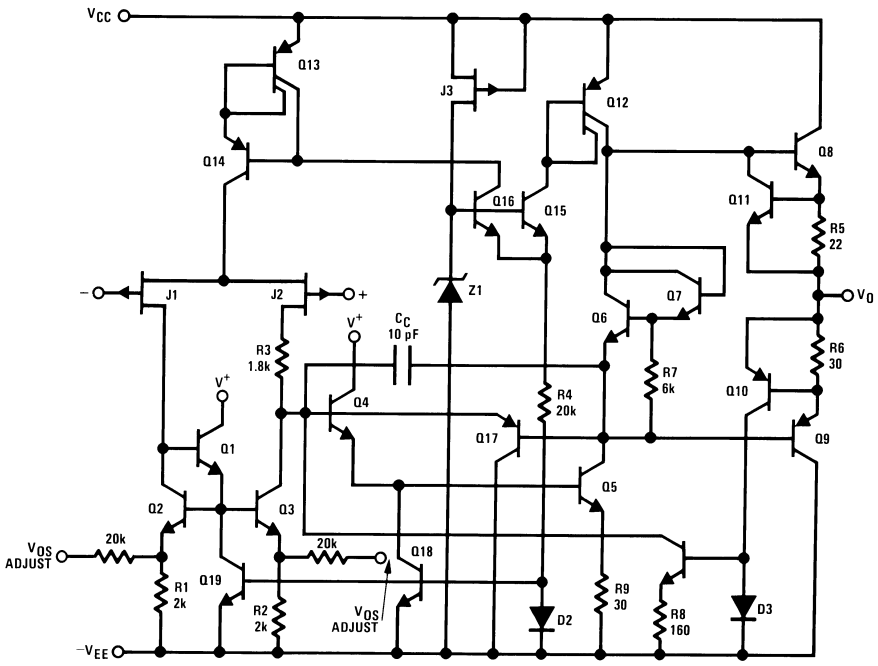


Figure 28. Detailed Schematic

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LF411 series of internally trimmed JFET input op amps (BI-FET II™) provide very low input offset voltage and input offset voltage drift. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore, large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltages. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

8.2 Typical Applications

1. High Speed Current Booster
2. 10-Bit Linear DAC with No V_{OS} Adjust
3. Single Supply Analog Switch with Buffered Output

8.2.1 High-Speed Current Booster

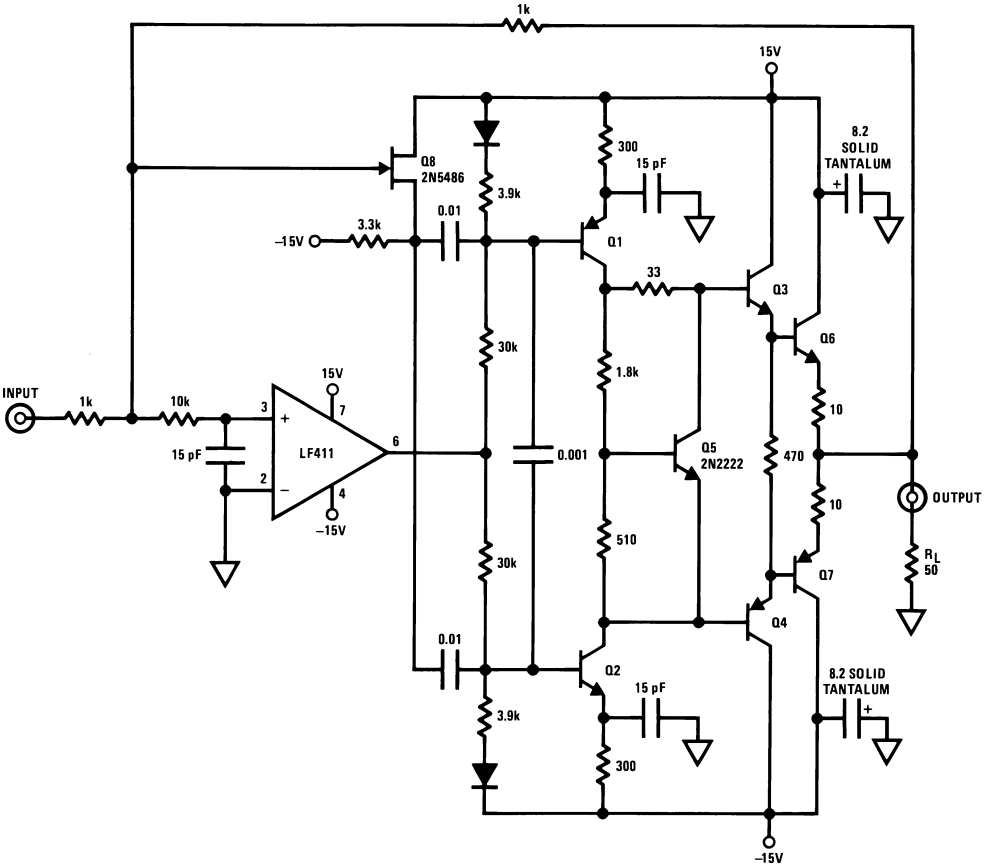


Figure 29. High-Speed Current Booster

Typical Applications (continued)

8.2.1.1 Design Requirements

PNP = 2N2905

NPN = 2N2219

TO-5 heat sinks for Q6-Q7

±15V supplies.

8.2.1.2 Detailed Design Procedure

Exceeding the negative common-mode limit on either input will force the output to a high state, potentially causing a reversal of phase to the output. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output; however, if both inputs exceed the limit, the output of the amplifier may be forced to a high state.

The amplifier will operate with a common-mode input voltage equal to the positive supply; however, the gain bandwidth and slew rate may be decreased in this condition. When the negative common-mode voltage swings to within 3V of the negative supply, an increase in input offset voltage may occur.

The LF411 is biased by a zener reference which allows normal circuit operation on ±4.5V power supplies. Supply voltages less than these may result in lower gain bandwidth and slew rate.

The LF411 will drive a 2 kΩ load resistance to ±10V over the full temperature range. If the amplifier is forced to drive heavier load currents, however, an increase in input offset voltage may occur on the negative voltage swing and finally reach an active current limit on both positive and negative swings.

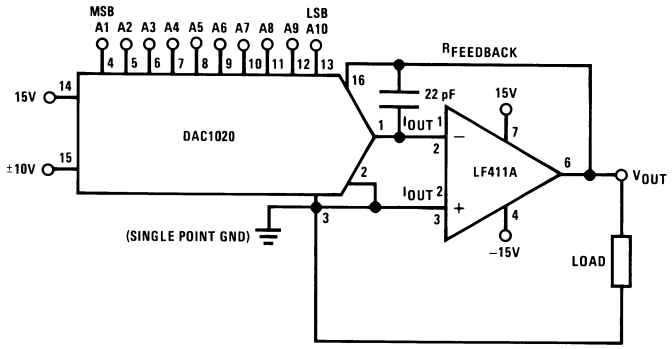
Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to AC ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately 6 times the expected 3 dB frequency, a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

Typical Applications (continued)

8.2.2 10-Bit Linear DAC with No V_{OS} Adjust



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \cdots \frac{A10}{1024}\right)$$

$$-10V \le V_{REF} \le 10V$$

$$0 \le V_{OUT} \le -\frac{1023}{1024}V_{REF}$$

where A_N=1 if the A_N digital input is high
A_N=0 if the A_N digital input is low

Figure 30. 10-Bit Linear DAC with No V_{OS} Adjust

8.2.2.1 Design Requirements

±15V supplies.

8.2.2.2 Detailed Design Procedure

See Section 9.2.1.2.

8.2.3 Single Supply Analog Switch With Buffered Output

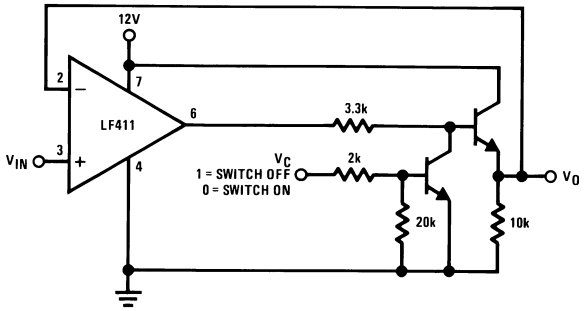


Figure 31. Single Supply Analog Switch With Buffered Output

8.2.3.1 Design Requirements

Single 12V supply.

8.2.3.2 Detailed Design Procedure

See Section 9.2.1.2.

9 Power Supply Recommendations

For proper operation, the power supplies must be properly decoupled. For decoupling the supply lines it is suggested that 0.1µF capacitors be placed as close as possible to the op amp power supply pins. The minimum power supply voltage is ±5V.

10 Layout

10.1 Layout Guidelines

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize “pick-up” and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

10.2 Layout Example

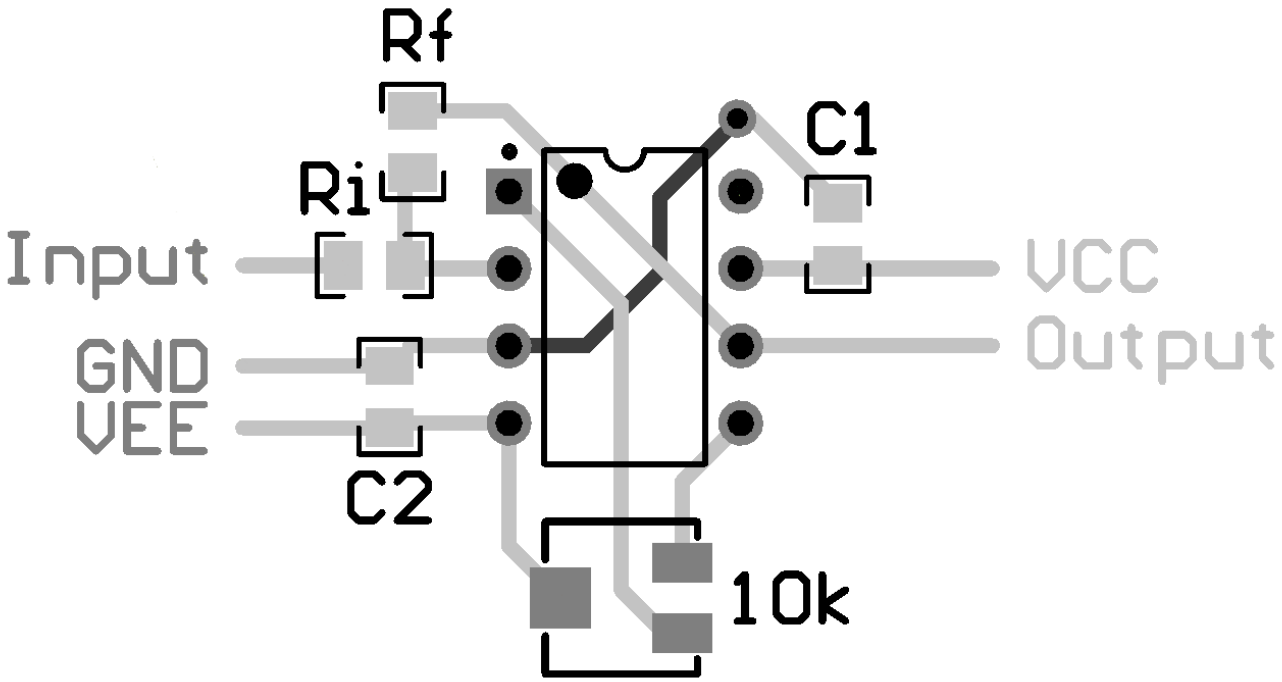


Figure 32. LF411-N Layout

11 Device and Documentation Support

11.1 Trademarks

All trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LF411ACN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	Call TI	Level-1-NA-UNLIM	0 to 70	LF 411ACN	Samples
LF411CN/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LF 411CN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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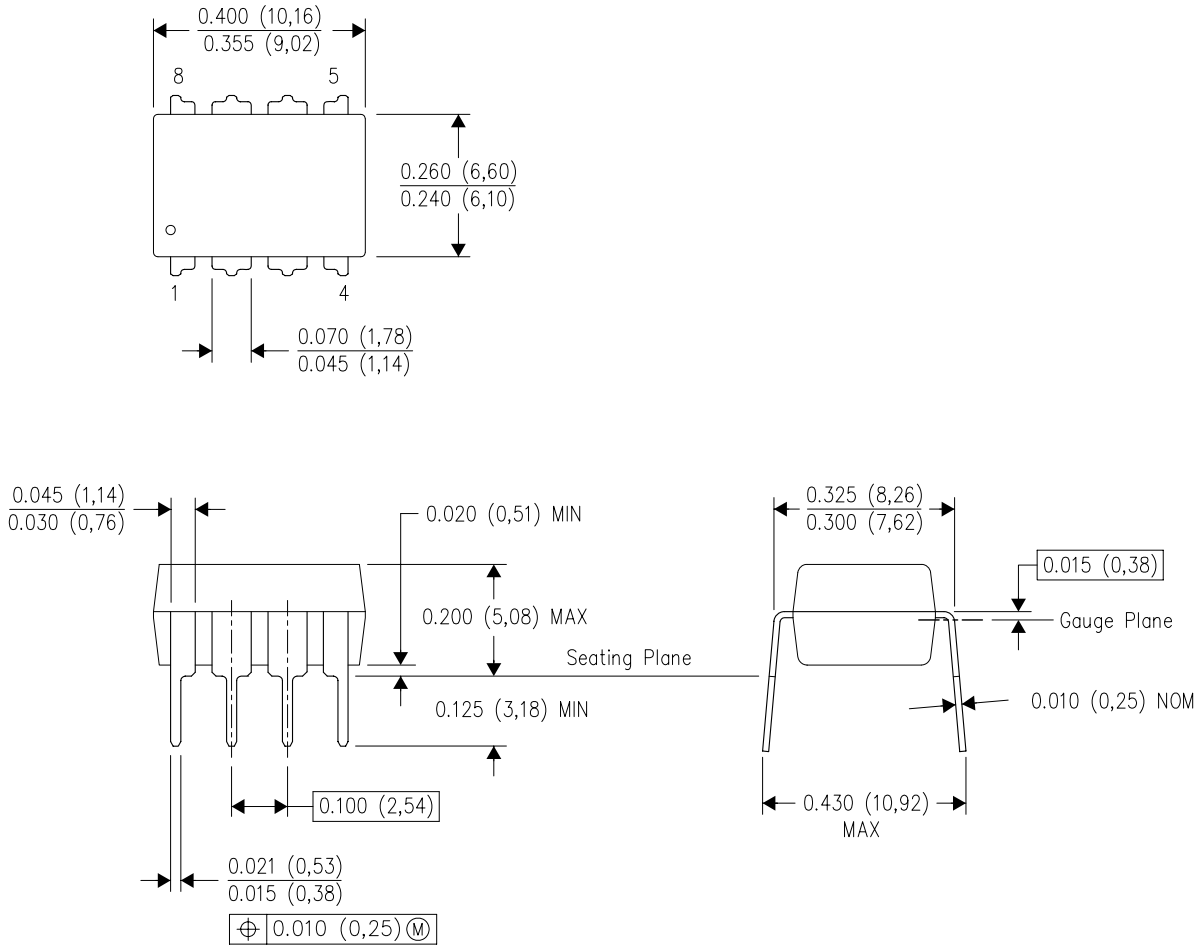
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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