

2SC3948

Silicon High Speed Power Transistor

2SC3948 500V, 10A

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Rating	Unit
Storage Temperature Range	T_{stg}		-55 ~ +150	°C
Junction Temperature	T_j		+150	°C
Collector to Base Voltage	V_{CBO}		850	V
Emitter to Base Voltage	V_{EBO}		7	V
Collector to Emitter Voltage	V_{CEO}		500	V
Collector Current	I_C		10	A
	I_{CM}	$P_W \leq 25\mu s, D.R. \leq 50\%$	15	
Base Current	I_B		4	A
Collector Power Dissipation	P_C	$T_C = 25^\circ C$	75	W

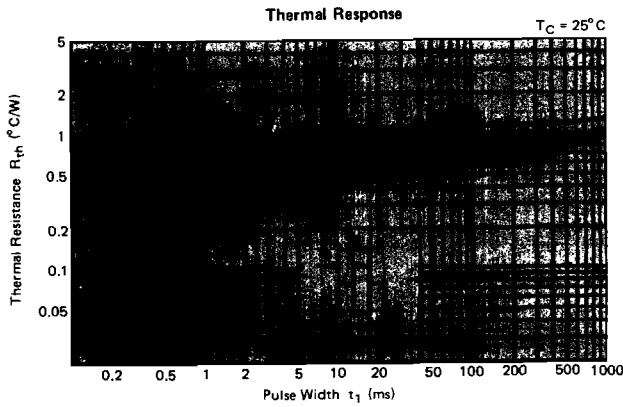
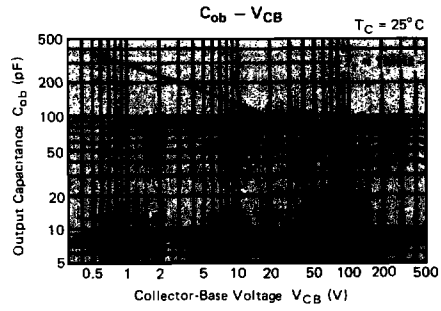
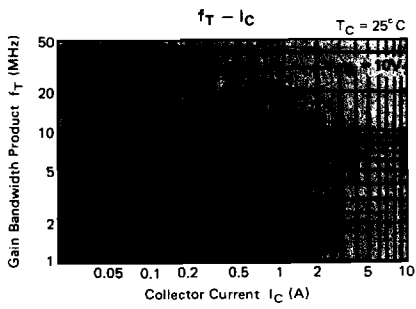
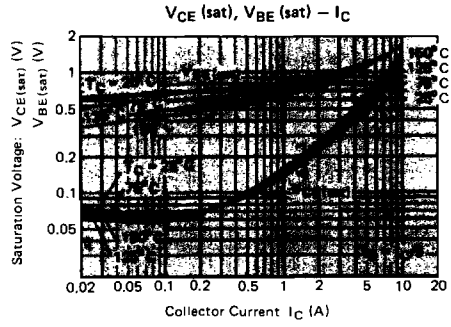
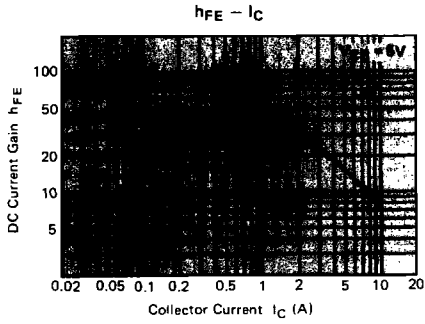
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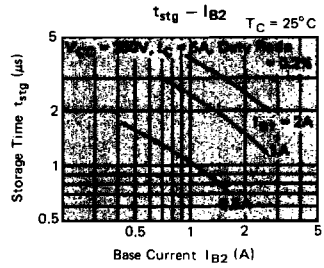
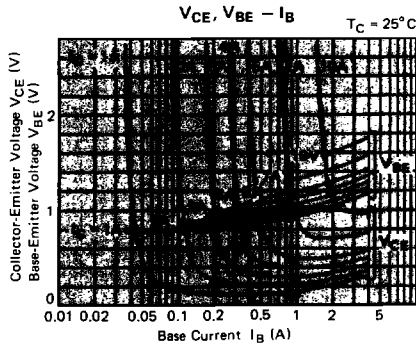
ELECTRICAL CHARACTERISTICS ($T_B = 25^\circ C$)

Parameter	Symbol	Test Conditions	Limit			Unit
			Min.	Typ.	Max.	
Collector to Base Breakdown Voltage	$V_{(BR)CBO}$	$I_C = 1mA, I_E = 0$	850	-	-	V
Emitter to Base Breakdown Voltage	$V_{(BR)EBO}$	$I_E = 1mA, I_C = 0$	7	-	-	V
Collector to Emitter Sustaining Voltage	$V_{(BR)CEO}$	$I_C = 10mA, R_{BE} = \infty\Omega$	500	-	-	V
Collector to Emitter Sustaining Voltage	$V_{CEX(SUS)}$	$I_C = 4A, I_{B2} = -2A, L = 200\mu H^*$	700	-	-	V
Collector Cutoff Current	I_{CBO}	$V_{CB} = 800V, I_E = 0$	-	-	100	μA
		$V_{CB} = 800V, I_E = 0, T_C = 100^\circ C$	-	-	1	mA
Emitter Cutoff Current	I_{EBO}	$V_{EB} = 6V, I_C = 0$	-	-	100	μA
DC Current Gain	h_{FE}	$V_{CE} = 5V, I_C = 5A^{**}$	10	15	30	-
Collector to Emitter Saturation Voltage	$V_{CE(sat)}$	$I_C = 5A, I_B = 1A^{**}$	-	0.5	1.0	V
Base to Emitter Saturation Voltage	$V_{BE(sat)}$		-	1.2	1.5	V
Output Capacitance	C_{ob}	$V_{CB} = 10V, I_E = 0, f = 1MHz$	-	130	-	pF
Gain Bandwidth Product	f_T	$V_{CE} = 10V, I_C = 1A$	-	20	-	MHz
Rise Time	t_r	$V_{CC} = 250V, I_C = 5A, 2I_{B1} = -I_{B2} = 2A^*$	-	0.18	0.5	μs
Storage Time	t_{stg}		-	1.50	2.5	μs
Fall Time	t_f		-	0.07	0.3	μs

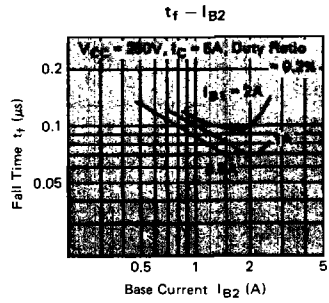
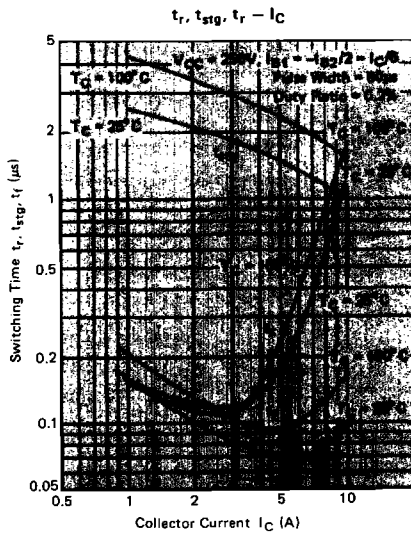
*1 Test Circuit **2 Pulse $P_W \leq 300\mu s$, Duty Ratio $\leq 6\%$

2

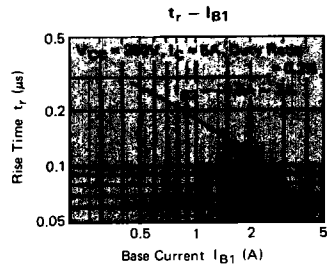
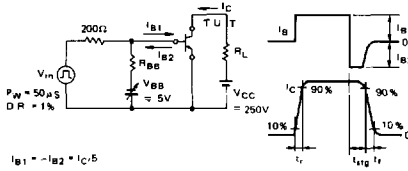




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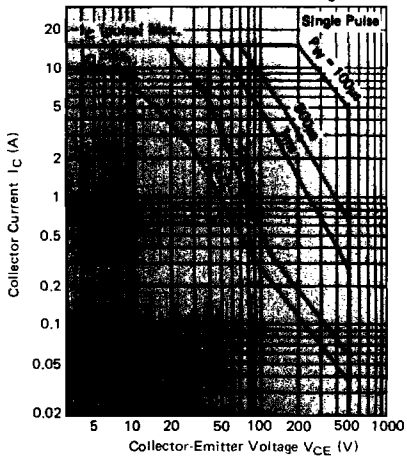
Test Circuit for Switching Time



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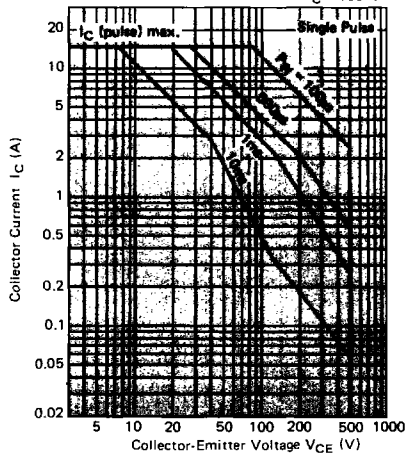
Forward Bias Safe Operating Area - 1

$T_C = 25^\circ\text{C}$

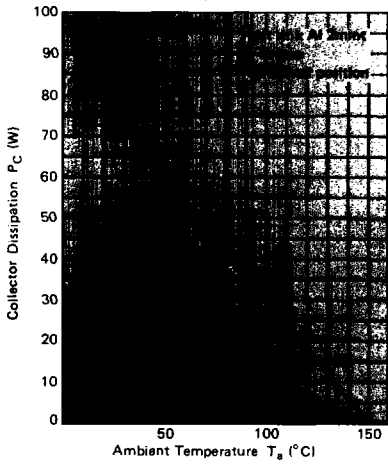


Forward Bias Safe Operating Area - 2

$T_C = 100^\circ\text{C}$

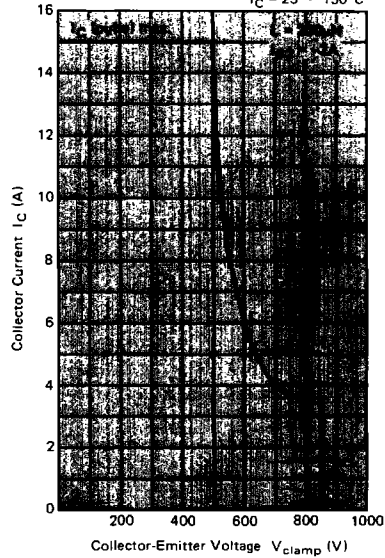


$P_C - T_a$



Reverse Bias Safe Operating Area

$T_C = 25 \sim 150^\circ\text{C}$



Test Circuit for $V_{CE(sus)}$ and Reverse Bias Safe Operating Area

