

# Z80-CPU Z80A-CPU



## Product Specification

The Zilog Z80 product line is a complete set of microcomputer components, development systems and support software. The Z80 microcomputer component set includes all of the circuits necessary to build high-performance microcomputer systems with virtually no other logic and a minimum number of low cost standard memory elements.

The Z80 and Z80A CPU's are third generation single chip microprocessors with unrivaled computational power. This increased computational power results in higher system through-put and more efficient memory utilization when compared to second generation microprocessors. In addition, the Z80 and Z80A CPU's are very easy to implement into a system because of their single voltage requirement plus all output signals are fully decoded and timed to control standard memory or peripheral circuits. The circuit is implemented using an N-channel, ion implanted, silicon gate MOS process.

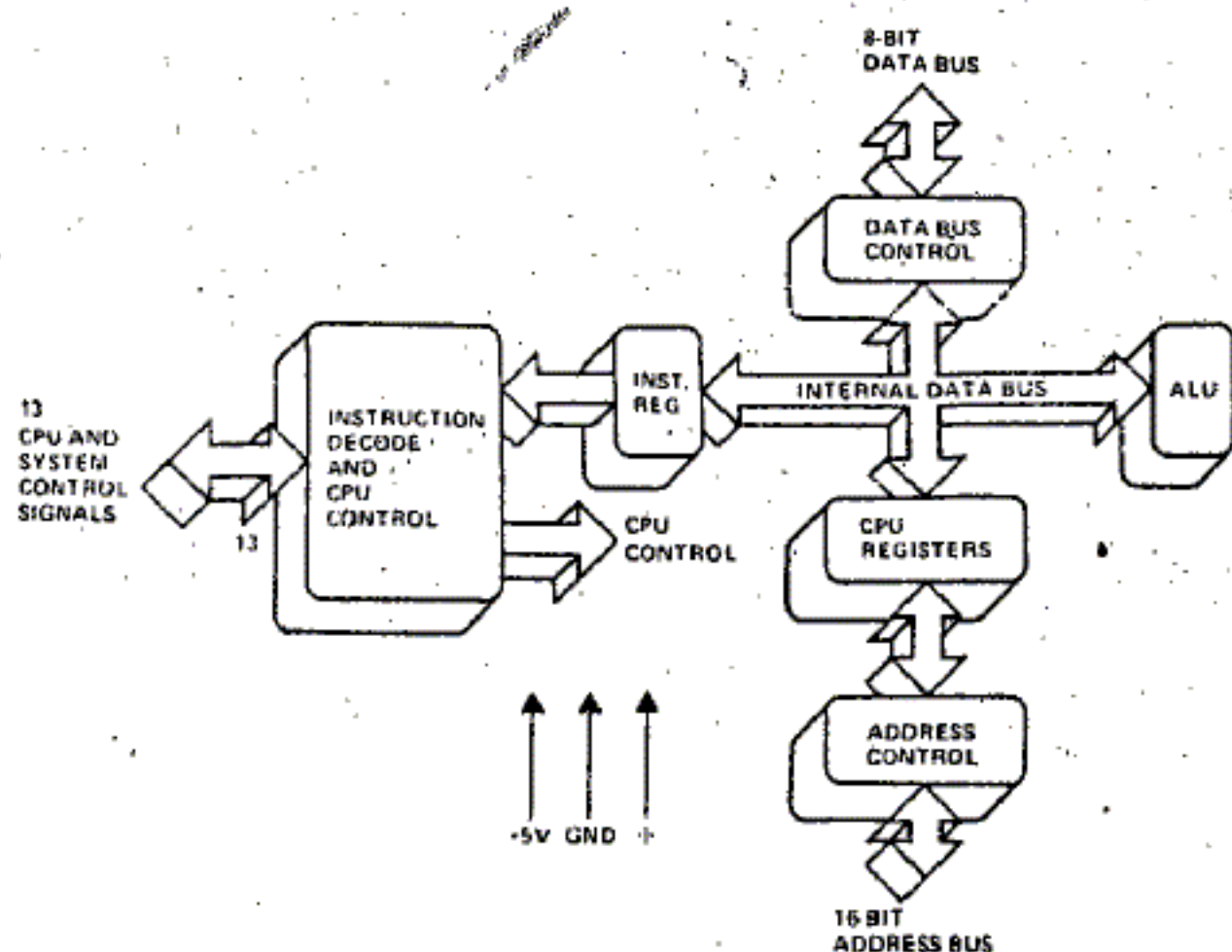
Figure 1 is a block diagram of the CPU, Figure 2 details the internal register configuration which contains 208 bits of Read/Write memory that are accessible to the programmer. The registers include two sets of six general purpose registers that may be used individually as 8-bit registers or as 16-bit register pairs. There are also two sets of accumulator and flag registers. The programmer has access to either set of main or alternate registers through a group of exchange instructions. This alternate set allows foreground/background mode of operation or may be reserved for very fast Interrupt response. Each CPU also contains a 16-bit stack pointer which permits simple implementation of

multiple level interrupts, unlimited subroutine nesting and simplification of many types of data handling.

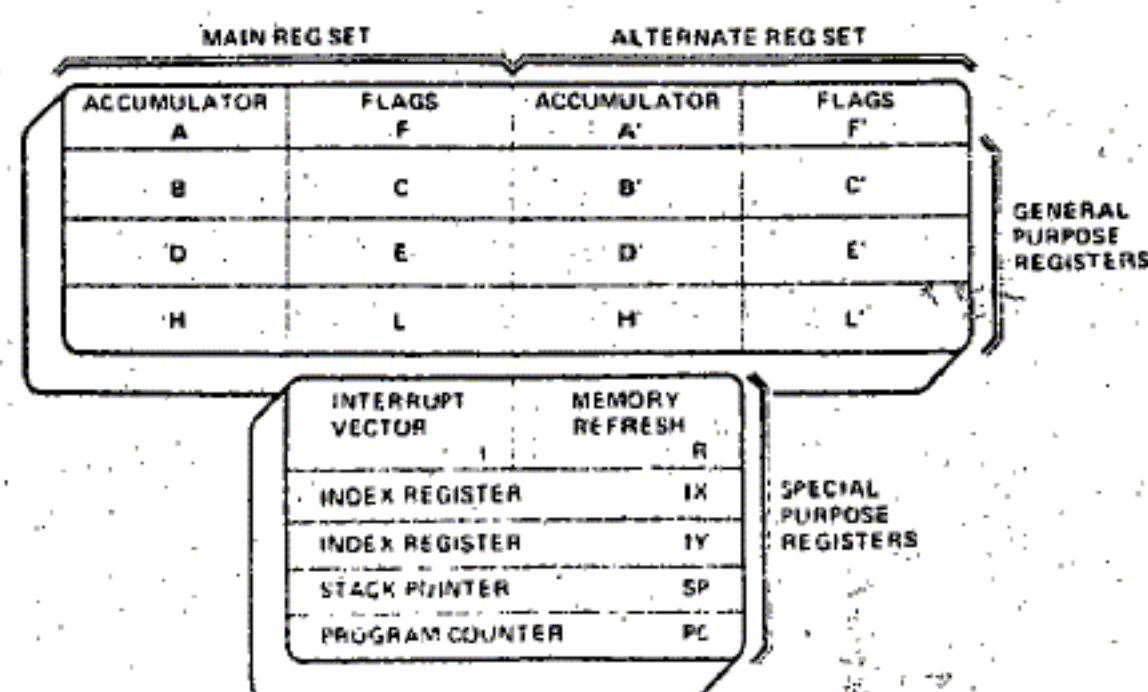
The two 16-bit index registers allow tabular data manipulation and easy implementation of relocatable code. The Refresh register provides for automatic, totally transparent refresh of external dynamic memories. The I register is used in a powerful interrupt response mode to form the upper 8 bits of a pointer to a interrupt service address table, while the interrupting device supplies the lower 8 bits of the pointer. An indirect call is then made to this service address.

### FEATURES

- Single chip, N-channel Silicon Gate CPU.
- 158 instructions—includes all 78 of the 8080A instructions with total software compatibility. New instructions include 4-, 8- and 16-bit operations with more useful addressing modes such as indexed, bit and relative.
- 17 internal registers.
- Three modes of fast interrupt response plus a non-maskable interrupt.
- Directly interfaces standard speed static or dynamic memories with virtually no external logic.
- 1.0  $\mu$ s instruction execution speed.
- Single 5 VDC supply and single-phase 5 volt Clock.
- Out-performs any other single chip microcomputer in 4-, 8-, or 16-bit applications.
- All pins TTL Compatible
- Built-in dynamic RAM refresh circuitry.



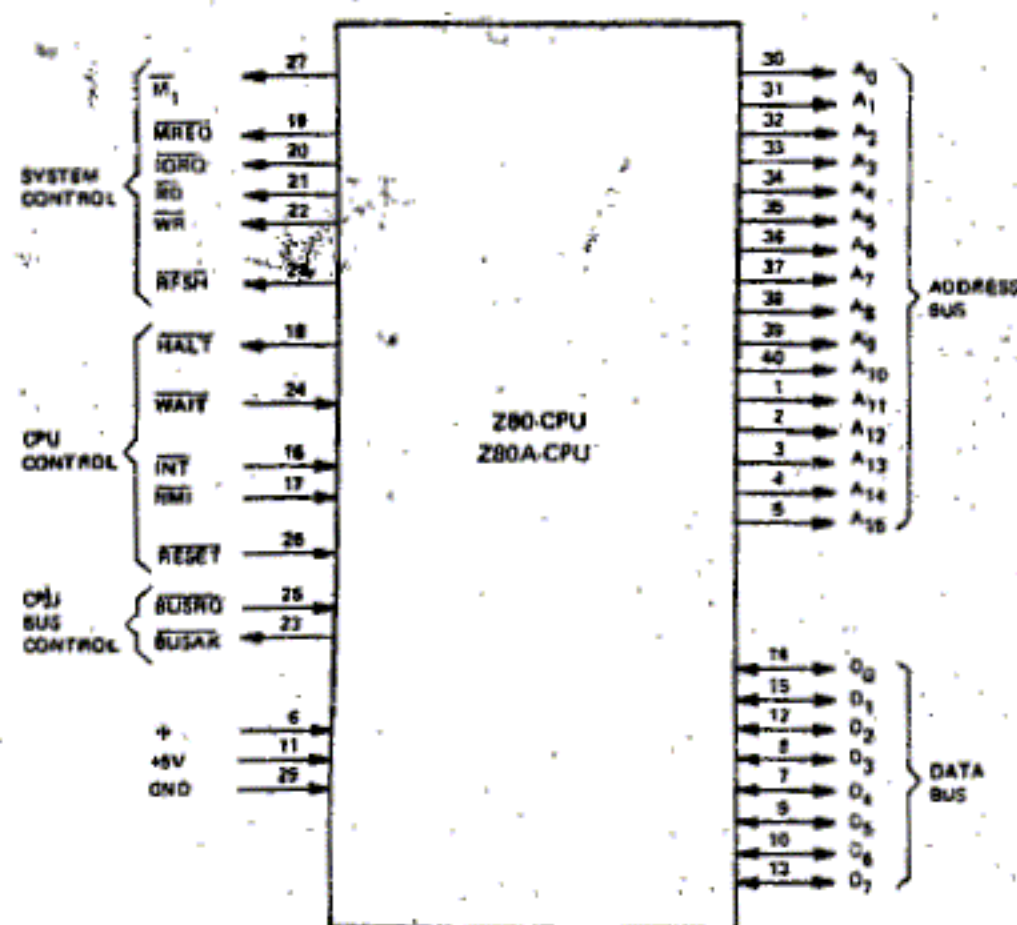
Z80, Z80A CPU BLOCK DIAGRAM



Z80, Z80A CPU REGISTERS



# Z80, Z80A-CPU Pin Description



**Z80, Z80A CPU PIN CONFIGURATION**

**A<sub>0</sub>-A<sub>15</sub>**  
(Address Bus)

Tri-state output, active high: A<sub>0</sub>-A<sub>15</sub> constitute a 16-bit address bus. The address bus provides the address for memory (up to 64K bytes) data exchanges and for I/O device data exchanges.

**D<sub>0</sub>-D<sub>7</sub>**  
(Data Bus)

Tri-state input/output, active high. D<sub>0</sub>-D<sub>7</sub> constitute an 8-bit bidirectional data bus. The data bus is used for data

**M<sub>1</sub>**  
(Machine Cycle one)

Output, active low.  $\overline{M_1}$  indicates that the current machine cycle is the OP code fetch cycle of an instruction execution.

**$\overline{MREQ}$**   
(Memory Request)

Tri-state output, active low. The memory request signal indicates that the address bus holds a valid address for a memory read or memory write operation.

**$\overline{IORQ}$**   
(Input/Output Request)

Tri-state output, active low. The  $\overline{IORQ}$  signal indicates that the lower half of the address bus holds a valid I/O address for a I/O read or write operation. An  $\overline{IORQ}$  signal is also generated when an interrupt is being acknowledged to indicate that an interrupt response vector can be placed on the data bus.

**$\overline{RD}$**   
(Memory Read)

Tri-state output, active low.  $\overline{RD}$  indicates that the CPU wants to read data from memory or an I/O device. The addressed I/O device or memory should use this signal to gate data onto the CPU data bus.

**$\overline{WR}$**   
(Memory Write)

Tri-state output, active low.  $\overline{WR}$  indicates that the CPU data bus holds valid data to be stored in the addressed memory or I/O device.

**$\overline{RFSH}$**   
(Refresh)

Output, active low.  $\overline{RFSH}$  indicates that the lower 7 bits of the address bus contain a refresh address for dynamic memories and the current  $\overline{MREQ}$  signal should be used to do a refresh read to all dynamic memories.

**$\overline{HALT}$**   
(Halt state)

Output, active low.  $\overline{HALT}$  indicates that the CPU has executed a HALT software instruction and is awaiting either a non-maskable or a maskable interrupt (with the mask enabled) before operation can resume. While halted, the CPU executes NOP's to maintain memory refresh activity.

**$\overline{WAIT}$**   
(Wait)

Input, active low.  $\overline{WAIT}$  indicates to the Z-80 CPU that the addressed memory or I/O devices are not ready for a data transfer. The CPU continues to enter wait states for as long as this signal is active.

**$\overline{INT}$**   
(Interrupt Request)

Input, active low. The Interrupt Request signal is generated by I/O devices. A request will be honored at the end of the current instruction if the internal software controlled interrupt enable flip-flop

**$\overline{NMI}$**   
(Non Maskable Interrupt)

Input, active low. The non-maskable interrupt request line has a higher priority than  $\overline{INT}$  and is always recognized at the end of the current instruction, independent of the status of the interrupt enable flip-flop.  $\overline{NMI}$  automatically forces the Z-80 CPU to restart to location 0066H.

**$\overline{RESET}$**

Input, active low.  $\overline{RESET}$  initializes the CPU as follows: reset interrupt enable flip-flop, clear PC and registers I and R and set interrupt to 8080A mode. During reset time, the address and data bus go to a high impedance state and all control output signals go to the inactive state.

**$\overline{BUSRQ}$**   
(Bus Request)

Input, active low. The bus request signal has a higher priority than  $\overline{NMI}$  and is always recognized at the end of the current machine cycle and is used to request the CPU address bus, data bus and tri-state output control signals to go to a high impedance state so that other devices can control these busses.

**$\overline{BUSAK}$**   
(Bus Acknowledge)

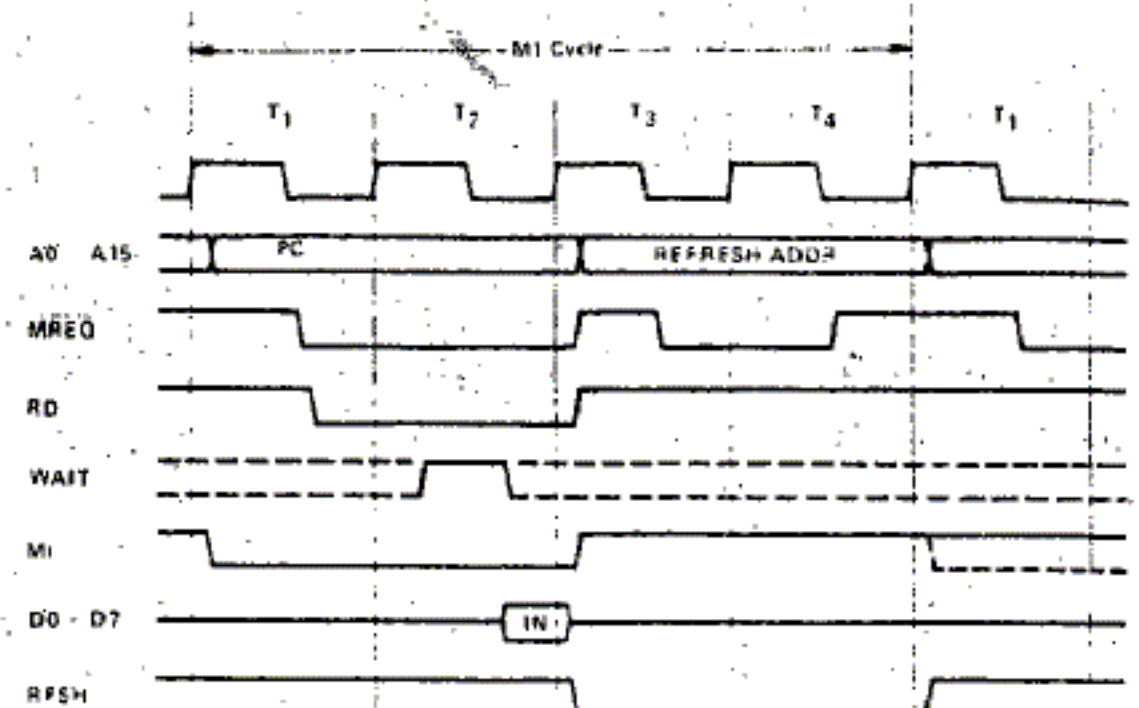
Output, active low. Bus acknowledge is used to indicate to the requesting device that the CPU address bus, data bus and tri-state control bus signals have been set to their high impedance state and the external device can now control these signals.



# Timing Waveforms

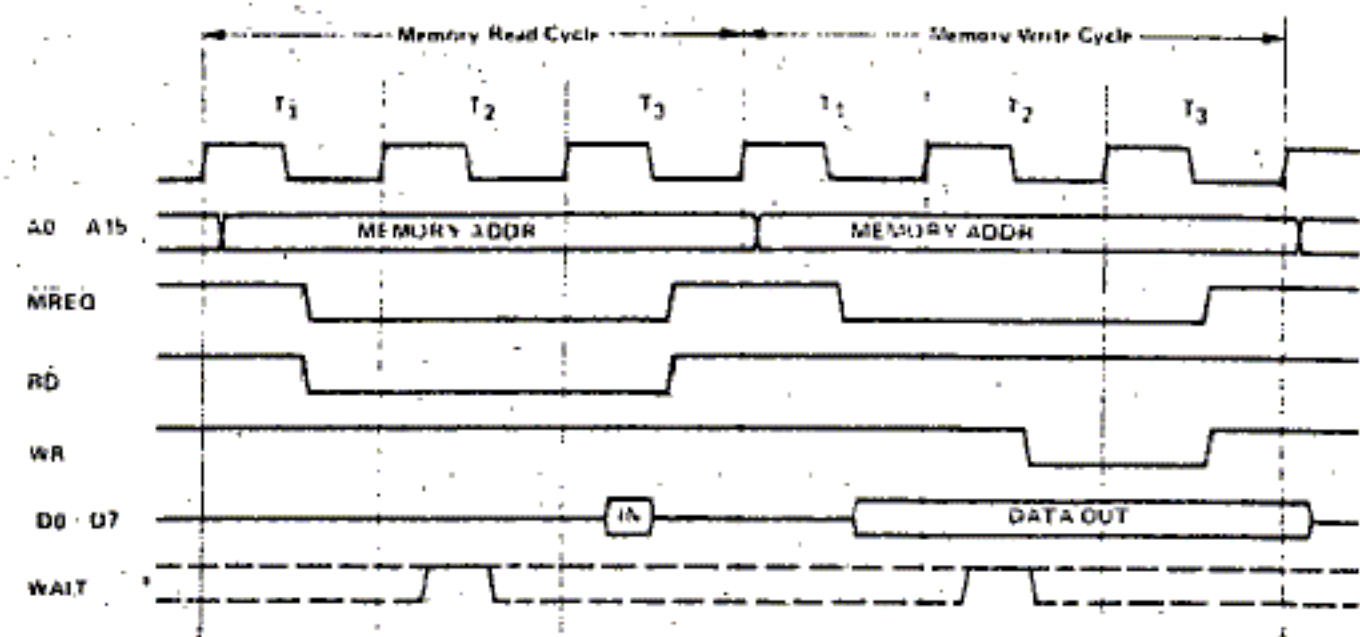
## INSTRUCTION OP CODE FETCH

The program counter content (PC) is placed on the address bus immediately at the start of the cycle. One half clock time later  $\overline{\text{MREQ}}$  goes active. The falling edge of  $\overline{\text{MREQ}}$  can be used directly as a chip enable to dynamic memories.  $\overline{\text{RD}}$  when active indicates that the memory data should be enabled onto the CPU data bus. The CPU samples data with the rising edge of the clock state  $T_3$ . Clock states  $T_3$  and  $T_4$  of a fetch cycle are used to refresh dynamic memories while the CPU is internally decoding and executing the instruction. The refresh control signal  $\overline{\text{RFSH}}$  indicates that a refresh read of all dynamic memories should be accomplished.



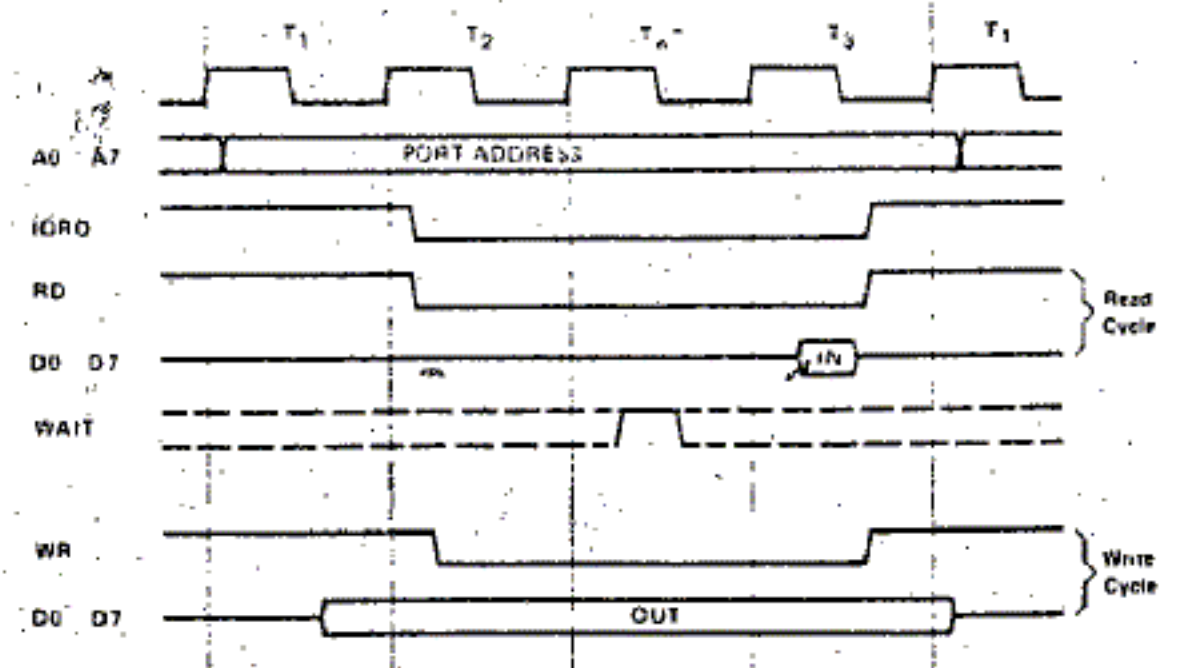
## MEMORY READ OR WRITE CYCLES

Illustrated here is the timing of memory read or write cycles other than an OP code fetch ( $M_1$  cycle). The  $\overline{\text{MREQ}}$  and  $\overline{\text{RD}}$  signals are used exactly as in the fetch cycle. In the case of a memory write cycle, the  $\overline{\text{MREQ}}$  also becomes active when the address bus is stable so that it can be used directly as a chip enable for dynamic memories. The  $\overline{\text{WR}}$  line is active when data on the data bus is stable so that it can be used directly as a R/W pulse to virtually any type of semiconductor memory.



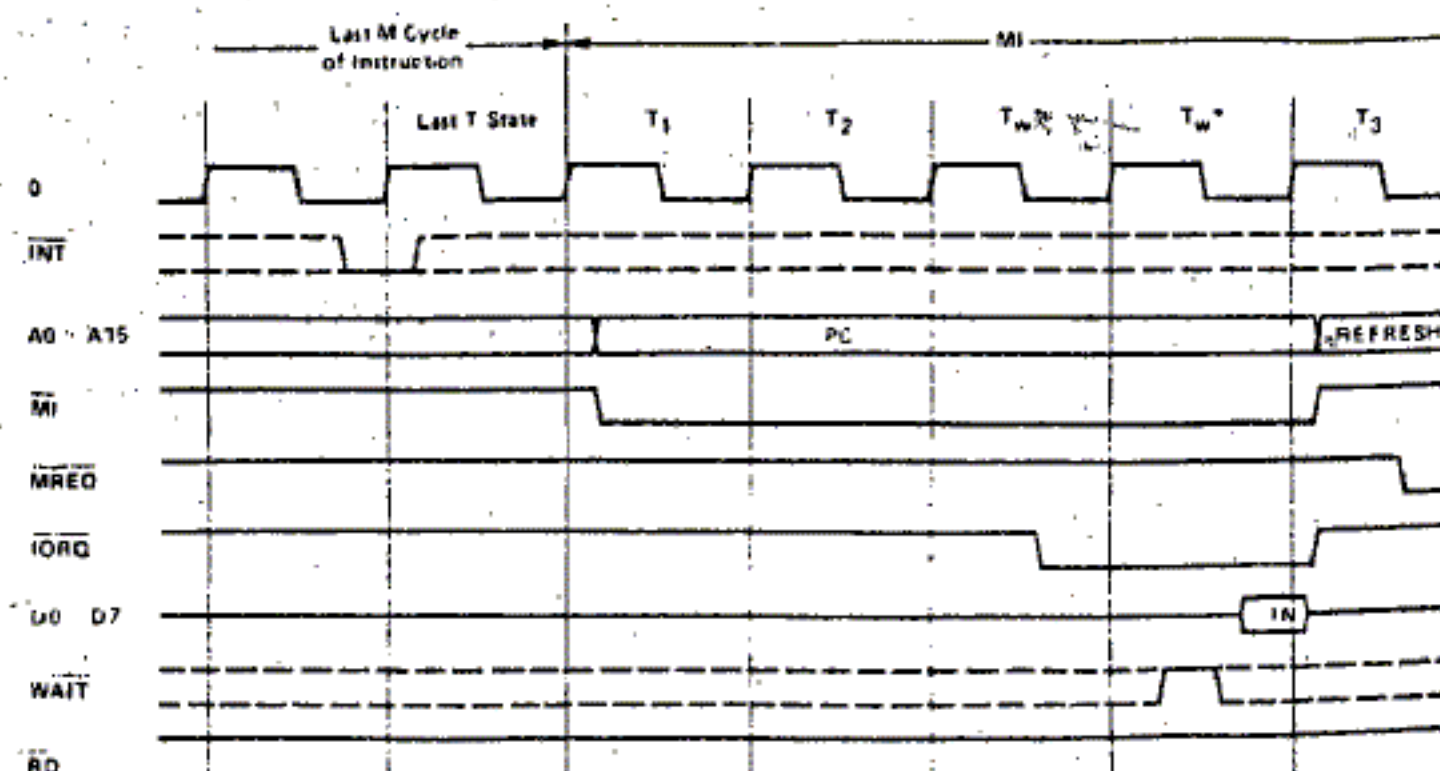
## INPUT OR OUTPUT CYCLES

Illustrated here is the timing for an I/O read or I/O write operation. Notice that during I/O operations a single wait state is automatically inserted ( $T_w^*$ ). The reason for this is that during I/O operations this extra state allows sufficient time for an I/O port to decode its address and activate the  $\overline{\text{WAIT}}$  line if a wait is required.



## INTERRUPT REQUEST/ACKNOWLEDGE CYCLE

The interrupt signal is sampled by the CPU with the rising edge of the last clock at the end of any instruction. When an interrupt is accepted, a special  $M_1$  cycle is generated. During this  $M_1$  cycle, the  $\overline{\text{IORQ}}$  signal becomes active (instead of  $\overline{\text{MREQ}}$ ) to indicate that the interrupting device can place an 8-bit vector on the data bus. Two wait states ( $T_w^*$ ) are automatically added to this cycle so that a ripple priority interrupt scheme, such as the one used in the Z80 peripheral controllers, can be easily implemented.





# Z80, Z80A Instruction Set

The following is a summary of the Z80, Z80A instruction set showing the assembly language mnemonic and the symbolic operation performed by the instruction. A more detailed listing appears in the Z80-CPU technical manual, and assembly language programming manual. The instructions are divided into the following categories:

|                                               |                         |
|-----------------------------------------------|-------------------------|
| 8-bit loads                                   | Miscellaneous Group     |
| 16-bit loads                                  | Rotates and Shifts      |
| Exchanges                                     | Bit Set, Reset and Test |
| Memory Block Moves                            | Input and Output        |
| Memory Block Searches                         | Jumps                   |
| 8-bit arithmetic and logic                    | Calls                   |
| 16-bit arithmetic                             | Restarts                |
| General purpose Accumulator & Flag Operations | Returns                 |

In the table the following terminology is used.

|    |                                                         |
|----|---------------------------------------------------------|
| b  | ≡ a bit number in any 8-bit register or memory location |
| cc | ≡ flag condition code                                   |
| NZ | ≡ non zero                                              |
| Z  | ≡ zero                                                  |
| NC | ≡ non carry                                             |
| C  | ≡ carry                                                 |
| PO | ≡ Parity odd or no over flow                            |
| PE | ≡ Parity even or over flow                              |
| P  | ≡ Positive                                              |
| M  | ≡ Negative (minus)                                      |

|                       |                                                                                                        |
|-----------------------|--------------------------------------------------------------------------------------------------------|
| d                     | ≡ any 8-bit destination register or memory location                                                    |
| dd                    | ≡ any 16-bit destination register or memory location                                                   |
| e                     | ≡ 8-bit signed 2's complement displacement used in relative jumps and indexed addressing               |
| L                     | ≡ 8 special call locations in page zero. In decimal notation these are 0, 8, 16, 24, 32, 40, 48 and 56 |
| n                     | ≡ any 8-bit binary number                                                                              |
| nn                    | ≡ any 16-bit binary number                                                                             |
| r                     | ≡ any 8-bit general purpose register (A, B, C, D, E, H, or L)                                          |
| s                     | ≡ any 8-bit source register or memory location                                                         |
| sb                    | ≡ a bit in a specific 8-bit register or memory location                                                |
| ss                    | ≡ any 16-bit source register or memory location                                                        |
| subscript "L"         | ≡ the low order 8 bits of a 16-bit register                                                            |
| subscript "H"         | ≡ the high order 8 bits of a 16-bit register                                                           |
| ( )                   | ≡ the contents within the ( ) are to be used as a pointer to a memory location or I/O port number      |
| 8-bit registers       | are A, B, C, D, E, H, L, I and R                                                                       |
| 16-bit register pairs | are AF, BC, DE and HL                                                                                  |
| 16-bit registers      | are SP, PC, IX and IY                                                                                  |

Addressing Modes implemented include combinations of the following:

|                    |                   |
|--------------------|-------------------|
| Immediate          | Indexed           |
| Immediate extended | Register          |
| Modified Page Zero | Implied           |
| Relative           | Register Indirect |
| Extended           | Bit               |

| Mnemonic    | Symbolic Operation                                                                                             | Comments                              |
|-------------|----------------------------------------------------------------------------------------------------------------|---------------------------------------|
| LD r, s     | $r \leftarrow s$                                                                                               | $s \equiv r, n, (HL), (IX+e), (IY+e)$ |
| LD d, r     | $d \leftarrow r$                                                                                               | $d \equiv (HL), r, (IX+e), (IY+e)$    |
| LD d, n     | $d \leftarrow n$                                                                                               | $d \equiv (HL), (IX+e), (IY+e)$       |
| LD A, s     | $A \leftarrow s$                                                                                               | $s \equiv (BC), (DE), (nn), I, R$     |
| LD d, A     | $d \leftarrow A$                                                                                               | $d \equiv (BC), (DE), (nn), I, R$     |
| LD dd, nn   | $dd \leftarrow nn$                                                                                             | $dd \equiv BC, DE, HL, SP, IX, IY$    |
| LD dd, (nn) | $dd \leftarrow (nn)$                                                                                           | $dd \equiv BC, DE, HL, SP, IX, IY$    |
| LD (nn), ss | $(nn) \leftarrow ss$                                                                                           | $ss \equiv BC, DE, HL, SP, IX, IY$    |
| LD SP, ss   | $SP \leftarrow ss$                                                                                             | $ss = HL, IX, IY$                     |
| PUSH ss     | $(SP-1) \leftarrow ss_H; (SP-2) \leftarrow ss_L$                                                               | $ss = BC, DE, HL, AF, IX, IY$         |
| POP dd      | $dd_L \leftarrow (SP); dd_H \leftarrow (SP+1)$                                                                 | $dd = BC, DE, HL, AF, IX, IY$         |
| EX DE, HL   | $DE \leftrightarrow HL$                                                                                        |                                       |
| EX AF, AF'  | $AF \leftrightarrow AF'$                                                                                       |                                       |
| EXX         | $\begin{pmatrix} BC \\ DE \\ HL \end{pmatrix} \leftrightarrow \begin{pmatrix} BC' \\ DE' \\ HL' \end{pmatrix}$ |                                       |
| EX (SP), ss | $(SP) \leftrightarrow ss_L, (SP+1) \leftrightarrow ss_H$                                                       | $ss \equiv HL, IX, IY$                |

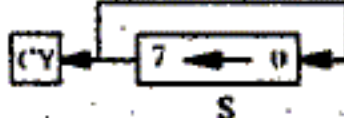
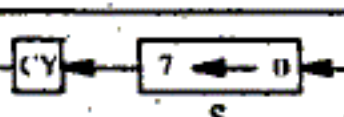
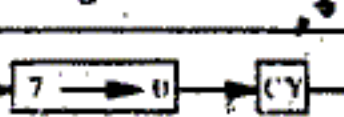
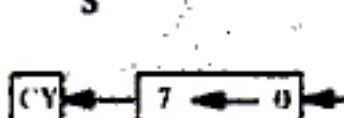
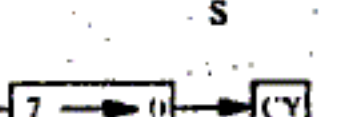
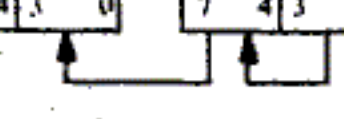
MEMORY BLOCK MOVES

MEMORY BLOCK SEARCHES

8-BIT ALU

| Mnemonic | Symbolic Operation                                                                                              | Comments                                          |
|----------|-----------------------------------------------------------------------------------------------------------------|---------------------------------------------------|
| LDI      | $(DE) \leftarrow (HL), DE \leftarrow DE+1$<br>$HL \leftarrow HL+1, BC \leftarrow BC-1$                          |                                                   |
| LDIR     | $(DE) \leftarrow (HL), DE \leftarrow DE+1$<br>$HL \leftarrow HL+1, BC \leftarrow BC-1$<br>Repeat until $BC = 0$ |                                                   |
| LDD      | $(DE) \leftarrow (HL), DE \leftarrow DE-1$<br>$HL \leftarrow HL-1, BC \leftarrow BC-1$                          |                                                   |
| LDDR     | $(DE) \leftarrow (HL), DE \leftarrow DE-1$<br>$HL \leftarrow HL-1, BC \leftarrow BC-1$<br>Repeat until $BC = 0$ |                                                   |
| CPI      | $A-(HL), HL \leftarrow HL+1$<br>$BC \leftarrow BC-1$                                                            |                                                   |
| CPIR     | $A-(HL), HL \leftarrow HL+1$<br>$BC \leftarrow BC-1$ . Repeat until $BC = 0$ or $A = (HL)$                      | $A-(HL)$ sets the flags only. $A$ is not affected |
| CPD      | $A-(HL), HL \leftarrow HL-1$<br>$BC \leftarrow BC-1$                                                            |                                                   |
| CPDR     | $A-(HL), HL \leftarrow HL-1$<br>$BC \leftarrow BC-1$ . Repeat until $BC = 0$ or $A = (HL)$                      |                                                   |
| ADD s    | $A \leftarrow A + s$                                                                                            |                                                   |
| ADC s    | $A \leftarrow A + s + CY$                                                                                       | $CY$ is the carry flag                            |
| SUB s    | $A \leftarrow A - s$                                                                                            |                                                   |
| SBC s    | $A \leftarrow A - s - CY$                                                                                       | $s \equiv r, n, (HL), (IX+e), (IY+e)$             |
| AND s    | $A \leftarrow A \wedge s$                                                                                       |                                                   |
| OR s     | $A \leftarrow A \vee s$                                                                                         |                                                   |
| XOR s    | $A \leftarrow A \oplus s$                                                                                       |                                                   |



| Mnemonic   | Symbolic Operation                                                                  | Comments                                                                                                                                                           |
|------------|-------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CP s       | $A \leftarrow s$                                                                    | $s = r, n \text{ (HL)}$<br>$(IX+e), (IY+e)$                                                                                                                        |
| INC d      | $d \leftarrow d + 1$                                                                | $d = r, \text{ (HL)}$<br>$(IX+e), (IY+e)$                                                                                                                          |
| DEC d      | $d \leftarrow d - 1$                                                                |                                                                                                                                                                    |
| ADD HL, ss | $HL \leftarrow HL + ss$                                                             | $ss \equiv BC, DE, HL, SP$<br>$ss \equiv BC, DE, IX, SP$<br>$ss \equiv BC, DE, IY, SP$<br>$dd \equiv BC, DE, HL, SP, IX, IY$<br>$dd \equiv BC, DE, HL, SP, IX, IY$ |
| ADC HL, ss | $HL \leftarrow HL + ss + CY$                                                        |                                                                                                                                                                    |
| SBC HL, ss | $HL \leftarrow HL - ss - CY$                                                        |                                                                                                                                                                    |
| ADD IX, ss | $IX \leftarrow IX + ss$                                                             |                                                                                                                                                                    |
| ADD IY, ss | $IY \leftarrow IY + ss$                                                             |                                                                                                                                                                    |
| INC dd     | $dd \leftarrow dd + 1$                                                              |                                                                                                                                                                    |
| DEC dd     | $dd \leftarrow dd - 1$                                                              |                                                                                                                                                                    |
| DAA        | Converts A contents into packed BCD following add or subtract.                      | Operands must be in packed BCD format                                                                                                                              |
| CPL        | $A \leftarrow \overline{A}$                                                         |                                                                                                                                                                    |
| NEG        | $A \leftarrow 00 - A$                                                               |                                                                                                                                                                    |
| CCF        | $CY \leftarrow \overline{CY}$                                                       |                                                                                                                                                                    |
| SCF        | $CY \leftarrow 1$                                                                   |                                                                                                                                                                    |
| NOP        | No operation                                                                        |                                                                                                                                                                    |
| HALT       | Halt CPU                                                                            |                                                                                                                                                                    |
| DI         | Disable Interrupts                                                                  |                                                                                                                                                                    |
| EI         | Enable Interrupts                                                                   |                                                                                                                                                                    |
| IM 0       | Set interrupt mode 0                                                                | 8080A mode<br>Call to 0038 <sub>H</sub><br>Indirect Call                                                                                                           |
| IM 1       | Set interrupt mode 1                                                                |                                                                                                                                                                    |
| IM 2       | Set interrupt mode 2                                                                |                                                                                                                                                                    |
| RLC s      |  | $s \equiv r, \text{ (HL)}$<br>$(IX+e), (IY+e)$                                                                                                                     |
| RL s       |  |                                                                                                                                                                    |
| RRC s      |  |                                                                                                                                                                    |
| RR s       |  |                                                                                                                                                                    |
| SLA s      |  |                                                                                                                                                                    |
| SRA s      |  |                                                                                                                                                                    |
| SRL s      |  |                                                                                                                                                                    |
| RLD        |  |                                                                                                                                                                    |
| RRD        |  |                                                                                                                                                                    |

| Mnemonic    | Symbolic Operation                                                                             | Comments                                                                                                                                    |
|-------------|------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
| BIT b, s    | $Z \leftarrow \overline{s_b}$                                                                  | Z is zero flag                                                                                                                              |
| SET b, s    | $s_b \leftarrow 1$                                                                             | $s \equiv r, \text{ (HL)}$                                                                                                                  |
| RES b, s    | $s_b \leftarrow 0$                                                                             | $(IX+e), (IY+e)$                                                                                                                            |
| IN A, (n)   | $A \leftarrow (n)$                                                                             | Set flags                                                                                                                                   |
| IN r, (C)   | $r \leftarrow (C)$                                                                             |                                                                                                                                             |
| INI         | $(HL) \leftarrow (C), HL \leftarrow HL + 1$<br>$B \leftarrow B - 1$                            |                                                                                                                                             |
| INIR        | $(HL) \leftarrow (C), HL \leftarrow HL + 1$<br>$B \leftarrow B - 1$<br>Repeat until $B = 0$    |                                                                                                                                             |
| IND         | $(HL) \leftarrow (C), HL \leftarrow HL - 1$<br>$B \leftarrow B - 1$                            |                                                                                                                                             |
| INDR        | $(HL) \leftarrow (C), HL \leftarrow HL - 1$<br>$B \leftarrow B - 1$<br>Repeat until $B = 0$    |                                                                                                                                             |
| OUT(n), A   | $(n) \leftarrow A$                                                                             |                                                                                                                                             |
| OUT(C), r   | $(C) \leftarrow r$                                                                             |                                                                                                                                             |
| OUTI        | $(C) \leftarrow (HL), HL \leftarrow HL + 1$<br>$B \leftarrow B - 1$                            |                                                                                                                                             |
| OTIR        | $(C) \leftarrow (HL), HL \leftarrow HL + 1$<br>$B \leftarrow B - 1$<br>Repeat-until $B = 0$    |                                                                                                                                             |
| OUTD        | $(C) \leftarrow (HL), HL \leftarrow HL - 1$<br>$B \leftarrow B - 1$                            | $cc \begin{cases} NZ & PO \\ Z & PE \\ NC & P \\ C & M \end{cases}$<br>$kk \begin{cases} NZ & NC \\ Z & C \end{cases}$<br>$ss = HL, IX, IY$ |
| OTDR        | $(C) \leftarrow (HL), HL \leftarrow HL - 1$<br>$B \leftarrow B - 1$<br>Repeat until $B = 0$    |                                                                                                                                             |
| JP nn       | $PC \leftarrow nn$                                                                             |                                                                                                                                             |
| JP cc, nn   | If condition cc is true<br>$PC \leftarrow nn$ , else continue                                  |                                                                                                                                             |
| JR e        | $PC \leftarrow PC + e$                                                                         |                                                                                                                                             |
| JR kk, e    | If condition kk is true<br>$PC \leftarrow PC + e$ , else continue                              |                                                                                                                                             |
| JP (ss)     | $PC \leftarrow ss$                                                                             |                                                                                                                                             |
| DJNZ e      | $B \leftarrow B - 1$ , if $B = 0$ continue, else $PC \leftarrow PC + e$                        |                                                                                                                                             |
| CALL nn     | $(SP-1) \leftarrow PC_H$<br>$(SP-2) \leftarrow PC_L, PC \leftarrow nn$                         |                                                                                                                                             |
| CALL cc, nn | If condition cc is false continue, else same as CALL nn                                        |                                                                                                                                             |
| RST L       | $(SP-1) \leftarrow PC_H$<br>$(SP-2) \leftarrow PC_L, PC_H \leftarrow 0$<br>$PC_L \leftarrow L$ |                                                                                                                                             |
| RET         | $PC_L \leftarrow (SP)$<br>$PC_H \leftarrow (SP+1)$                                             | $cc \begin{cases} NZ & PO \\ Z & PE \\ NC & P \\ C & M \end{cases}$                                                                         |
| RET cc      | If condition cc is false continue, else same as RET                                            |                                                                                                                                             |
| RETI        | Return from interrupt, same as RET                                                             |                                                                                                                                             |
| RETN        | Return from non-maskable interrupt                                                             |                                                                                                                                             |

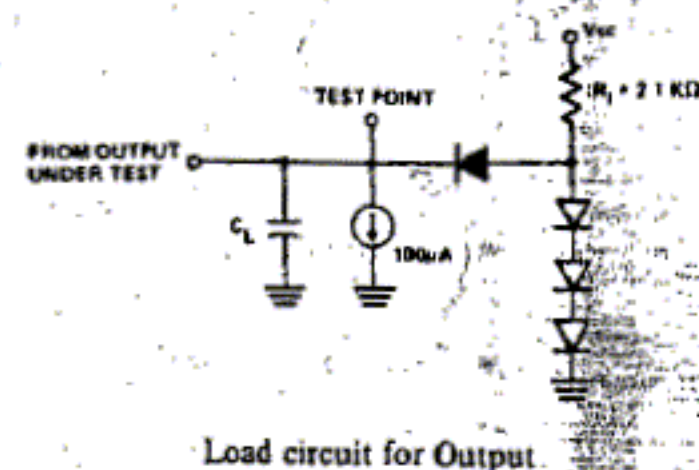


$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = +5V \pm 5\%$ , Unless Otherwise Noted.

| Signal                        | Symbol                      | Parameter                                                                                          | Min | Max  | Unit            | Test Condition       |
|-------------------------------|-----------------------------|----------------------------------------------------------------------------------------------------|-----|------|-----------------|----------------------|
| $\Phi$                        | $t_c$                       | Clock Period                                                                                       | 4   | 112  | $\mu\text{sec}$ |                      |
|                               | $t_{w(\Phi H)}$             | Clock Pulse Width, Clock High                                                                      | 180 | 15   | nsec            |                      |
|                               | $t_{w(\Phi L)}$             | Clock Pulse Width, Clock Low                                                                       | 180 | 2000 | nsec            |                      |
|                               | $t_r, t_f$                  | Clock Rise and Fall Time                                                                           |     | 30   | nsec            |                      |
| $A_{0-15}$                    | $t_D(AD)$                   | Address Output Delay                                                                               |     | 145  | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_F(AD)$                   | Delay to Float                                                                                     |     | 110  | nsec            |                      |
|                               | $t_{acm}$                   | Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)                                           | 11  |      | nsec            |                      |
|                               | $t_{aci}$                   | Address Stable Prior to $\overline{IORQ}$ , $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)         | 12  |      | nsec            |                      |
|                               | $t_{ca}$                    | Address Stable from $\overline{RD}$ or $\overline{WR}$                                             | 13  |      | nsec            |                      |
| $D_{0-7}$                     | $t_D(D)$                    | Data Output Delay                                                                                  |     | 260  | nsec            | $C_L = 200\text{pF}$ |
|                               | $t_F(D)$                    | Delay to Float During Write Cycle                                                                  |     | 90   | nsec            |                      |
|                               | $t_{SD}(D)$                 | Data Setup Time to Rising Edge of Clock During M1 Cycle                                            | 50  |      | nsec            |                      |
|                               | $t_{SD}(D)$                 | Data Setup Time to Falling Edge of Clock During M2 to M5                                           | 60  |      | nsec            |                      |
|                               | $t_{dcm}$                   | Data Stable Prior to $\overline{WR}$ (Memory Cycle)                                                | 15  |      | nsec            |                      |
|                               | $t_{dci}$                   | Data Stable Prior to $\overline{WR}$ (I/O Cycle)                                                   | 16  |      | nsec            |                      |
|                               | $t_{cdf}$                   | Data Stable From $\overline{WR}$                                                                   | 17  |      | nsec            |                      |
|                               | $t_H$                       | Any Hold Time for Setup Time                                                                       | 0   |      | nsec            |                      |
| $\overline{MREQ}$             | $t_{DL\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low                          |     | 100  | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_{DH\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High                          |     | 100  | nsec            |                      |
|                               | $t_{DL\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High                         |     | 100  | nsec            |                      |
|                               | $t_w(\overline{MRL})$       | Pulse Width, $\overline{MREQ}$ Low                                                                 | 18  |      | nsec            |                      |
|                               | $t_w(\overline{MRH})$       | Pulse Width, $\overline{MREQ}$ High                                                                | 19  |      | nsec            |                      |
| $\overline{IORQ}$             | $t_{DL\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low                           |     | 90   | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_{DL\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low                          |     | 110  | nsec            |                      |
|                               | $t_{DH\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High                          |     | 100  | nsec            |                      |
|                               | $t_{DH\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High                         |     | 110  | nsec            |                      |
|                               |                             |                                                                                                    |     |      |                 |                      |
| $\overline{RD}$               | $t_{DL\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low                               |     | 100  | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_{DL\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low                              |     | 130  | nsec            |                      |
|                               | $t_{DH\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High                              |     | 100  | nsec            |                      |
|                               | $t_{DH\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High                             |     | 110  | nsec            |                      |
|                               |                             |                                                                                                    |     |      |                 |                      |
| $\overline{WR}$               | $t_{DL\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low                               |     | 80   | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_{DL\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low                              |     | 90   | nsec            |                      |
|                               | $t_{DH\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High                             |     | 100  | nsec            |                      |
|                               | $t_w(\overline{WRL})$       | Pulse Width, $\overline{WR}$ Low                                                                   | 110 |      | nsec            |                      |
|                               |                             |                                                                                                    |     |      |                 |                      |
| $\overline{MI}$               | $t_{DL}(\overline{MI})$     | $\overline{MI}$ Delay From Rising Edge of Clock, $\overline{MI}$ Low                               |     | 130  | nsec            | $C_L = 30\text{pF}$  |
|                               | $t_{DH}(\overline{MI})$     | $\overline{MI}$ Delay From Rising Edge of Clock, $\overline{MI}$ High                              |     | 130  | nsec            |                      |
| $\overline{RFSH}$             | $t_{DL}(\overline{RF})$     | $\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low                           |     | 180  | nsec            | $C_L = 30\text{pF}$  |
|                               | $t_{DH}(\overline{RF})$     | $\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High                          |     | 150  | nsec            |                      |
| $\overline{WAIT}$             | $t_s(\overline{WT})$        | $\overline{WAIT}$ Setup Time to Falling Edge of Clock                                              | 70  |      | nsec            |                      |
| $\overline{HALT}$             | $t_D(\overline{HT})$        | $\overline{HALT}$ Delay Time From Falling Edge of Clock                                            |     | 300  | nsec            | $C_L = 50\text{pF}$  |
| $\overline{INT}$              | $t_s(\overline{IT})$        | $\overline{INT}$ Setup Time to Rising Edge of Clock                                                | 80  |      | nsec            |                      |
| $\overline{NMI}$              | $t_w(\overline{NML})$       | Pulse Width, $\overline{NMI}$ Low                                                                  | 80  |      | nsec            |                      |
| $\overline{BUSRQ}$            | $t_s(\overline{BQ})$        | $\overline{BUSRQ}$ Setup Time to Rising Edge of Clock                                              | 80  |      | nsec            |                      |
| $\overline{BUSA\overline{K}}$ | $t_{DL}(\overline{BA})$     | $\overline{BUSA\overline{K}}$ Delay From Rising Edge of Clock, $\overline{BUSA\overline{K}}$ Low   |     | 120  | nsec            | $C_L = 50\text{pF}$  |
|                               | $t_{DH}(\overline{BA})$     | $\overline{BUSA\overline{K}}$ Delay From Falling Edge of Clock, $\overline{BUSA\overline{K}}$ High |     | 110  | nsec            |                      |
| $\overline{RESET}$            | $t_s(\overline{RS})$        | $\overline{RESET}$ Setup Time to Rising Edge of Clock                                              | 90  |      | nsec            |                      |
|                               | $t_F(C)$                    | Delay to Float ( $\overline{MREQ}$ , $\overline{IORQ}$ , $\overline{RD}$ and $\overline{WR}$ )     |     | 100  | nsec            |                      |
|                               | $t_{mr}$                    | $\overline{MI}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)                                 | 111 |      | nsec            |                      |

## NOTES:

- Data should be enabled onto the CPU data bus when  $\overline{RD}$  is active. During interrupt acknowledge data should be enabled when  $\overline{MI}$  and  $\overline{IORQ}$  are both active.
- All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- The  $\overline{RESET}$  signal must be active for a minimum of 3 clock cycles.
- Output Delay vs. Loaded Capacitance  
 $T_A = 70^\circ\text{C}$   $V_{CC} = +5V \pm 5\%$   
 (1)  $\Delta C_L = +100\text{pF}$  ( $A_0 - A_{15}$  and Control Signals), add 30 ns to timing shown.
- Although static by design, testing guarantees  $t_{w(\Phi H)}$  of 200  $\mu\text{sec}$  maximum



$$[12] t_{cdf} = t_{w(\Phi L)} + t_r + t_f$$

$$[1] t_{acm} = t_{w(\Phi H)} + t_r - 75$$

$$[2] t_{aci} = t_c - 80$$

$$[3] t_{ca} = t_{w(\Phi L)} + t_r - 40$$

$$[4] t_{caf} = t_{w(\Phi L)} + t_r - 60$$

$$[5] t_{dcm} = t_c - 180$$

$$[6] t_{dci} = t_{w(\Phi L)} + t_r - 180$$

$$[7] t_{cdf} = t_{w(\Phi L)} + t_r - 50$$

$$[8] t_w(\overline{MRL}) = t_c - 40$$

$$[9] t_w(\overline{MRH}) = t_{w(\Phi H)} + t_r - 30$$

$$[10] t_w(\overline{WR}) = t_c - 40$$

$$[11] t_{mr} = 2t_c + t_{w(\Phi H)} + t_r - 80$$







# Absolute Maximum Ratings

Temperature Under Bias  
Storage Temperature  
Voltage On Any Pin  
with Respect to Ground  
Power Dissipation

Specified operating range  
-65°C to +150°C  
-0.3V to +7V  
1.5W

## \*Comment

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: For Z80-CPU, all AC and DC characteristics remain the same for the military grade parts except  $I_{CC}$ .

$$I_{CC} = 200 \text{ mA}$$

## Z80-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$  unless otherwise specified

| Symbol    | Parameter                                 | Min.           | Typ. | Max.     | Unit          | Test Condition                     |
|-----------|-------------------------------------------|----------------|------|----------|---------------|------------------------------------|
| $V_{ILC}$ | Clock Input Low Voltage                   | -0.3           |      | 0.45     | V             |                                    |
| $V_{IHC}$ | Clock Input High Voltage                  | $V_{CC} - 0.2$ |      | $V_{CC}$ | V             |                                    |
| $V_{IL}$  | Input Low Voltage                         | -0.3           |      | 0.8      | V             |                                    |
| $V_{IH}$  | Input High Voltage                        | 2.0            |      | $V_{CC}$ | V             |                                    |
| $V_{OL}$  | Output Low Voltage                        |                |      | 0.4      | V             | $I_{OL} = 1.8 \text{ mA}$          |
| $V_{OH}$  | Output High Voltage                       | 2.4            |      |          | V             | $I_{OH} = -250 \mu\text{A}$        |
| $I_{CC}$  | Power Supply Current                      |                |      | 150      | mA            | $t_c = 400 \text{ nsec}$           |
| $I_{LI}$  | Input Leakage Current                     |                |      | 10       | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$    |
| $I_{LOH}$ | Tri-State Output Leakage Current in Float |                |      | 10       | $\mu\text{A}$ | $V_{OUT} = 2.4 \text{ to } V_{CC}$ |
| $I_{LOL}$ | Tri-State Output Leakage Current in Float |                |      | -10      | $\mu\text{A}$ | $V_{OUT} = 0.4 \text{ V}$          |
| $I_{ED}$  | Data Bus Leakage Current in Input Mode    |                |      | $\pm 10$ | $\mu\text{A}$ | $0 \leq V_{IN} \leq V_{CC}$        |

## Capacitance

$T_A = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ ,

unmeasured pins returned to ground

| Symbol    | Parameter          | Max. | Unit |
|-----------|--------------------|------|------|
| $C_\phi$  | Clock Capacitance  | 35   | pF   |
| $C_{IN}$  | Input Capacitance  | 5    | pF   |
| $C_{OUT}$ | Output Capacitance | 10   | pF   |

## Z80-CPU

### Ordering Information

C - Ceramic

P - Plastic

S - Standard  $5V \pm 5\%$   $0^\circ$  to  $70^\circ\text{C}$

E - Extended  $5V \pm 5\%$   $-40^\circ$  to  $85^\circ\text{C}$

M - Military  $5V \pm 10\%$   $-55^\circ$  to  $125^\circ\text{C}$

## Z80A-CPU D.C. Characteristics

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$  unless otherwise specified

| Symbol    | Parameter                                 | Min.           | Typ. | Max.     | Unit          | Test Condition                     |
|-----------|-------------------------------------------|----------------|------|----------|---------------|------------------------------------|
| $V_{ILC}$ | Clock Input Low Voltage                   | -0.3           |      | 0.45     | V             |                                    |
| $V_{IHC}$ | Clock Input High Voltage                  | $V_{CC} - 0.2$ |      | $V_{CC}$ | V             |                                    |
| $V_{IL}$  | Input Low Voltage                         | -0.3           |      | 0.8      | V             |                                    |
| $V_{IH}$  | Input High Voltage                        | 2.0            |      | $V_{CC}$ | V             |                                    |
| $V_{OL}$  | Output Low Voltage                        |                |      | 0.4      | V             | $I_{OL} = 1.8 \text{ mA}$          |
| $V_{OH}$  | Output High Voltage                       | 2.4            |      |          | V             | $I_{OH} = -250 \mu\text{A}$        |
| $I_{CC}$  | Power Supply Current                      |                | 90   | 200      | mA            | $t_c = 250 \text{ nsec}$           |
| $I_{LI}$  | Input Leakage Current                     |                |      | 10       | $\mu\text{A}$ | $V_{IN} = 0 \text{ to } V_{CC}$    |
| $I_{LOH}$ | Tri-State Output Leakage Current in Float |                |      | 10       | $\mu\text{A}$ | $V_{OUT} = 2.4 \text{ to } V_{CC}$ |
| $I_{LOL}$ | Tri-State Output Leakage Current in Float |                |      | -10      | $\mu\text{A}$ | $V_{OUT} = 0.4 \text{ V}$          |
| $I_{ED}$  | Data Bus Leakage Current in Input Mode    |                |      | $\pm 10$ | $\mu\text{A}$ | $0 \leq V_{IN} \leq V_{CC}$        |

## Capacitance

$T_A = 25^\circ\text{C}$ ,  $f = 1 \text{ MHz}$ ,

unmeasured pins returned to ground

| Symbol    | Parameter          | Max. | Unit |
|-----------|--------------------|------|------|
| $C_\phi$  | Clock Capacitance  | 35   | pF   |
| $C_{IN}$  | Input Capacitance  | 5    | pF   |
| $C_{OUT}$ | Output Capacitance | 10   | pF   |

## Z80A-CPU

### Ordering Information

C - Ceramic

P - Plastic

S - Standard  $5V \pm 5\%$   $0^\circ$  to  $70^\circ\text{C}$



$T_A = 0^\circ\text{C to } 70^\circ\text{C}$ ,  $V_{CC} = +5\text{V} \pm 5\%$ . Unless Otherwise Noted.

| Signal             | Symbol                      | Parameter                                                                                      | Min  | Max  | Unit            | Test Condition      |
|--------------------|-----------------------------|------------------------------------------------------------------------------------------------|------|------|-----------------|---------------------|
| $\Phi$             | $t_c$                       | Clock Period                                                                                   | .25  | 112  | $\mu\text{sec}$ |                     |
|                    | $t_w(\Phi H)$               | Clock Pulse Width, Clock High                                                                  | 110  | 1E   | nsec            |                     |
|                    | $t_w(\Phi L)$               | Clock Pulse Width, Clock Low                                                                   | 110  | 2000 | nsec            |                     |
|                    | $t_r, t_f$                  | Clock Rise and Fall Time                                                                       |      | 30   | nsec            |                     |
| $A_{0-15}$         | $t_D(AD)$                   | Address Output Delay                                                                           |      | 110  | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_F(AD)$                   | Delay to Float                                                                                 |      | 90   | nsec            |                     |
|                    | $t_{acm}$                   | Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)                                       | [1]  |      | nsec            |                     |
|                    | $t_{aci}$                   | Address Stable Prior to $\overline{IORQ}$ , $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)     | [2]  |      | nsec            |                     |
|                    | $t_{ca}$                    | Address Stable From $\overline{RD}$ , $\overline{WR}$ , $\overline{IORQ}$ or $\overline{MREQ}$ | [3]  |      | nsec            |                     |
|                    | $t_{caf}$                   | Address Stable From $\overline{RD}$ or $\overline{WR}$ During Float                            | [4]  |      | nsec            |                     |
| $D_{0-7}$          | $t_D(D)$                    | Data Output Delay                                                                              |      | 150  | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_F(D)$                    | Delay to Float During Write Cycle                                                              |      | 90   | nsec            |                     |
|                    | $t_{SD}(D)$                 | Data Setup Time to Rising Edge of Clock During M1 Cycle                                        | 35   |      | nsec            |                     |
|                    | $t_{SD}(D)$                 | Data Setup Time to Falling Edge of Clock During M2 to M5                                       | 50   |      | nsec            |                     |
|                    | $t_{dcm}$                   | Data Stable Prior to $\overline{WR}$ (Memory Cycle)                                            | [5]  |      | nsec            |                     |
|                    | $t_{dci}$                   | Data Stable Prior to $\overline{WR}$ (I/O Cycle)                                               | [6]  |      | nsec            |                     |
|                    | $t_{cdf}$                   | Data Stable From $\overline{WR}$                                                               | [7]  |      | nsec            |                     |
|                    | $t_H$                       | Any Hold Time for Setup Time                                                                   |      | 0    | nsec            |                     |
| $\overline{MREQ}$  | $t_{DL\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ Low                      |      | 85   | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DH\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Rising Edge of Clock, $\overline{MREQ}$ High                      |      | 85   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{MR})$ | $\overline{MREQ}$ Delay From Falling Edge of Clock, $\overline{MREQ}$ High                     |      | 85   | nsec            |                     |
|                    | $t_w(\overline{MRL})$       | Pulse Width, $\overline{MREQ}$ Low                                                             | [8]  |      | nsec            |                     |
|                    | $t_w(\overline{MRH})$       | Pulse Width, $\overline{MREQ}$ High                                                            | [9]  |      | nsec            |                     |
| $\overline{IORQ}$  | $t_{DL\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ Low                       |      | 75   | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DL\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ Low                      |      | 85   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Rising Edge of Clock, $\overline{IORQ}$ High                      |      | 85   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{IR})$ | $\overline{IORQ}$ Delay From Falling Edge of Clock, $\overline{IORQ}$ High                     |      | 85   | nsec            |                     |
|                    |                             |                                                                                                |      |      |                 |                     |
| $\overline{RD}$    | $t_{DL\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ Low                           |      | 85   | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DL\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ Low                          |      | 95   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Rising Edge of Clock, $\overline{RD}$ High                          |      | 85   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{RD})$ | $\overline{RD}$ Delay From Falling Edge of Clock, $\overline{RD}$ High                         |      | 85   | nsec            |                     |
|                    |                             |                                                                                                |      |      |                 |                     |
| $\overline{WR}$    | $t_{DL\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Rising Edge of Clock, $\overline{WR}$ Low                           |      | 65   | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DL\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ Low                          |      | 80   | nsec            |                     |
|                    | $t_{DH\Phi}(\overline{WR})$ | $\overline{WR}$ Delay From Falling Edge of Clock, $\overline{WR}$ High                         |      | 80   | nsec            |                     |
|                    | $t_w(\overline{WRL})$       | Pulse Width, $\overline{WR}$ Low                                                               | [10] |      | nsec            |                     |
| $\overline{M1}$    | $t_{DL}(\overline{M1})$     | $\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ Low                           |      | 100  | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DH}(\overline{M1})$     | $\overline{M1}$ Delay From Rising Edge of Clock, $\overline{M1}$ High                          |      | 100  | nsec            |                     |
| $\overline{RFSH}$  | $t_{DL}(\overline{RF})$     | $\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ Low                       |      | 130  | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DH}(\overline{RF})$     | $\overline{RFSH}$ Delay From Rising Edge of Clock, $\overline{RFSH}$ High                      |      | 120  | nsec            |                     |
| $\overline{WAIT}$  | $t_s(\overline{WT})$        | $\overline{WAIT}$ Setup Time to Falling Edge of Clock                                          | 70   |      | nsec            |                     |
| $\overline{HALT}$  | $t_D(\overline{HT})$        | $\overline{HALT}$ Delay Time From Falling Edge of Clock                                        |      | 300  | nsec            | $C_L = 50\text{pF}$ |
| $\overline{INT}$   | $t_s(\overline{IT})$        | $\overline{INT}$ Setup Time to Rising Edge of Clock                                            | 80   |      | nsec            |                     |
| $\overline{NMI}$   | $t_w(\overline{NML})$       | Pulse Width, $\overline{NMI}$ Low                                                              | 80   |      | nsec            |                     |
| $\overline{BUSRQ}$ | $t_s(\overline{BQ})$        | $\overline{BUSRQ}$ Setup Time to Rising Edge of Clock                                          | 50   |      | nsec            |                     |
| $\overline{BUSAK}$ | $t_{DL}(\overline{BA})$     | $\overline{BUSAK}$ Delay From Rising Edge of Clock, $\overline{BUSAK}$ Low                     |      | 100  | nsec            | $C_L = 50\text{pF}$ |
|                    | $t_{DH}(\overline{BA})$     | $\overline{BUSAK}$ Delay From Falling Edge of Clock, $\overline{BUSAK}$ High                   |      | 100  | nsec            |                     |
| $\overline{RESET}$ | $t_s(\overline{RS})$        | $\overline{RESET}$ Setup Time to Rising Edge of Clock                                          | 60   |      | nsec            |                     |
|                    | $t_F(C)$                    | Delay to Float ( $\overline{MREQ}$ , $\overline{IORQ}$ , $\overline{RD}$ and $\overline{WR}$ ) |      | 80   | nsec            |                     |
|                    | $t_{mr}$                    | M1 Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)                                          | [11] |      | nsec            |                     |

$$[12] t_c = t_w(\Phi H) + t_w(\Phi L) + t_r + t_f$$

$$[1] t_{acm} = t_w(\Phi H) + t_f - 65$$

$$[2] t_{aci} = t_c - 70$$

$$[3] t_{ca} = t_w(\Phi L) + t_f - 50$$

$$[4] t_{caf} = t_w(\Phi L) + t_f - 45$$

$$[5] t_{dcm} = t_c - 170$$

$$[6] t_{dci} = t_w(\Phi L) + t_f - 170$$

$$[7] t_{cdf} = t_w(\Phi L) + t_f - 70$$

$$[8] t_w(\overline{MRL}) = t_c - 30$$

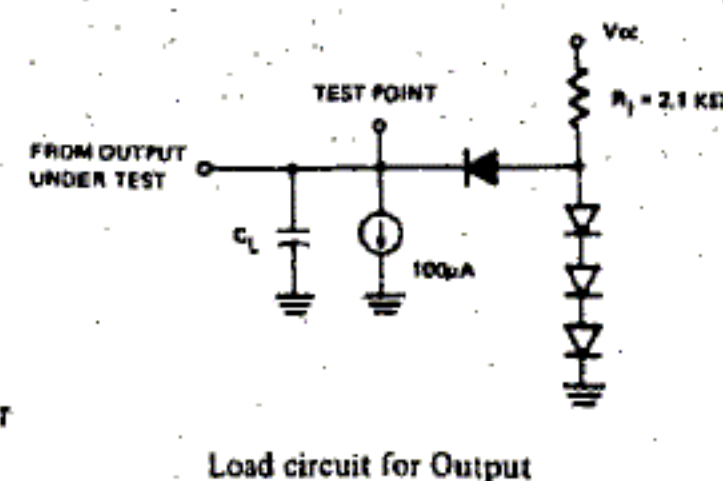
$$[9] t_w(\overline{MRH}) = t_w(\Phi H) + t_f - 20$$

$$[10] t_w(\overline{WRL}) = t_c - 30$$

$$[11] t_{mr} = 2t_c + t_w(\Phi H) + t_f - 65$$

## NOTES:

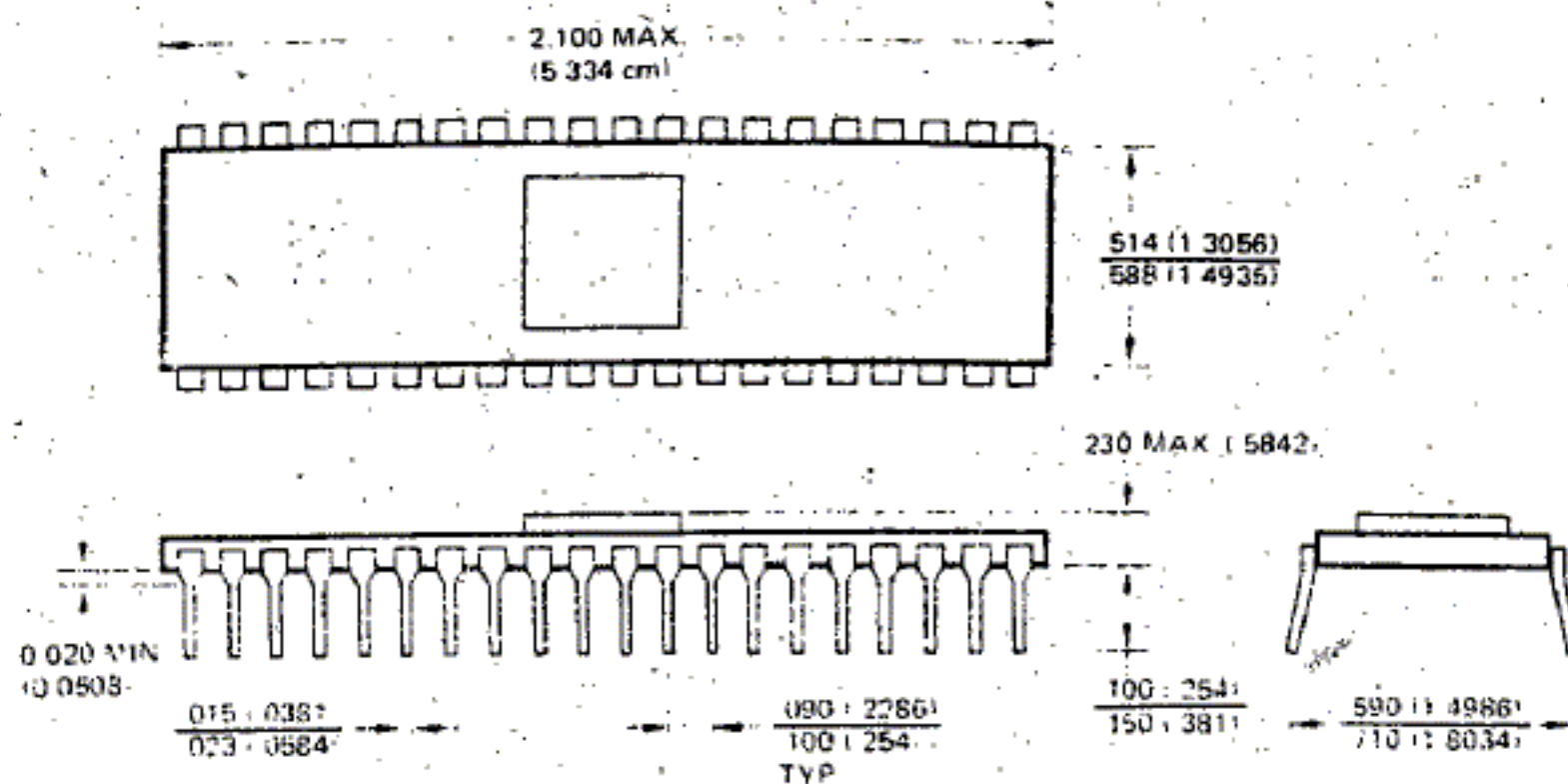
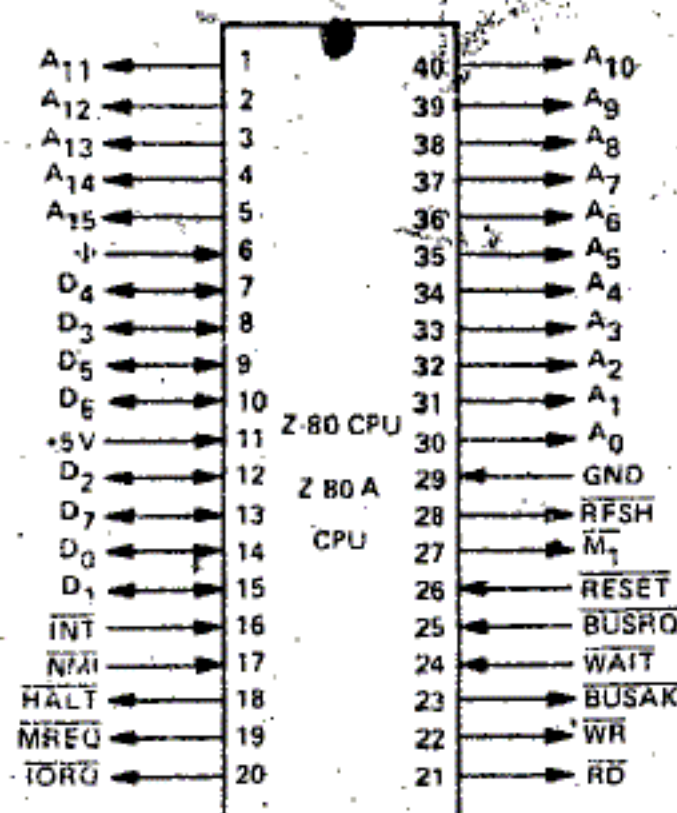
- Data should be enabled onto the CPU data bus when  $\overline{RD}$  is active. During interrupt acknowledge data should be enabled when  $\overline{M1}$  and  $\overline{IORQ}$  are both active.
- All control signals are internally synchronized, so they may be totally asynchronous with respect to the clock.
- The  $\overline{RESET}$  signal must be active for a minimum of 3 clock cycles.
- Output Delay vs. Loaded Capacitance  
 $T_A = 70^\circ\text{C}$   $V_{CC} = +5\text{V} \pm 5\%$   
 Add 10nsec delay for each 50pf increase in load up to maximum of 200pf for data bus and 100pf for address & control lines.
- Although static by design, testing guarantees  $t_w(\Phi H)$  of 200  $\mu\text{sec}$  maximum





## Package Configuration

## Package Outline



\*Dimensions for metric system are in parentheses

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