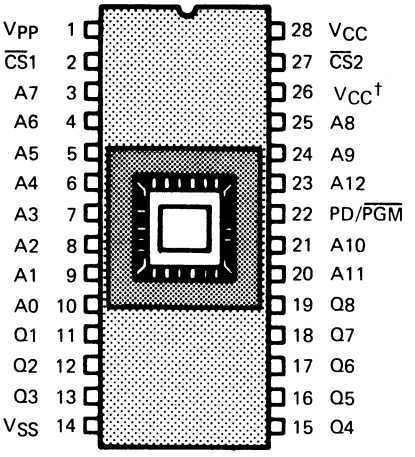
TMS 2564-45 JL
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

MAY 1981—REVISED MAY 1982

- Organization . . . 8K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation:

  Active . . . 400 mW Typical
  Standby . . . 75 mW Typical

TMS 2564
28-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



†V_{CC} may be connected to pin 26 for 24-pin ROM compatibility.

PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$(N)	Chip Selects
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2564 is a 65,536-bit, ultraviolet-light-erasable, electrically programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 2564 is offered in a dual-in-line ceramic package (JL or JDL suffix)* rated for operation from 0°C to 70°C.

Since this EPROM operates from a single +5 V supply (in the read mode), it is ideal for use in microprocessor systems. One other supply (+25 V) is needed for programming. Programming requires a single TTL level pulse per location. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

The TMS 2564 is compatible with other 5-volt ROMs and EPROMs, including those in a 24-pin package.

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operation

FUNCTION (PINS)	MODE								
	Read	Output Disable			Power Down	Start Programming	Inhibit Programming		
PD/$\overline{PGM}$ (22)	V_{IL}	V_{IH}	X	X	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}	X	X
$\overline{CS1}$ (21)	V_{IL}	X	V_{IH}	X	X	V_{IL}	X	V_{IH}	X
$\overline{CS2}$ (27)	V_{IL}	X	X	V_{IH}	X	V_{IL}	X	X	V_{IH}
V_{PP} (1)	+5 V	+5 V			+5 V	+25 V	+25 V		
V_{CC}* (26/28)	+5 V	+5 V			+5 V	+5 V	+5 V		
Q (11 to 13, 15 to 19)	Q	HI-Z			HI-Z	D	HI-Z		

X—Don't care.
* Do not use the internal jumper of 26-28 to conduct PC board currents.

read/output disable

When the outputs of two or more TMS 2564's are paralled on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS 2564, the low-level signal is applied to the PD/$\overline{PGM}$ and $\overline{CS}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8. Data can be accessed in 450 ns = $t_{a(A)}$.

power down

Active power dissipation can be cut by over 80 percent by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2564 is erased by exposing the chip through the transparent lid to high intensity ultraviolet (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

start programming

After erasure (all bits in logic high state), logic "0's" are programmed into the desired locations. A low can be erased only by ultraviolet light. The programming mode is achieved when Vpp is 25 V. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 50 millisecond low TTL pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More than one TMS 2564 can be programmed when the devices are connected in parallel. During programming both chip select signals should be held low unless program inhibit is desired.

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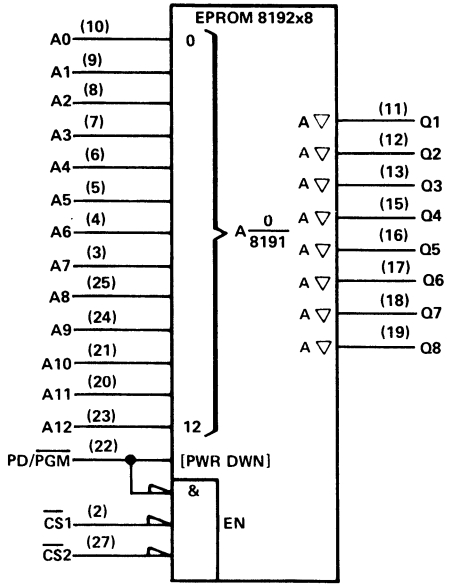
inhibit programming

When two or more TMS 2564's are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2564's not intended to be programmed should have a high level applied to PD/$\overline{PGM}$ or $\overline{CS1}$ or $\overline{CS2}$.

logic symbol†



† This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and recent decisions by IEEE and IEC. See explanation on page 289.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}		V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		V_{CC}+1	V
Low-level input voltage, V_{IL}	–0.1†		0.8	V
Read cycle time, $t_{c(rd)}$	450			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1V).

† The algebraic convention, where the more negative limit is designated as minimum, is used in this data sheet for logic voltage levels and time intervals.

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electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS 2564			UNIT
			MIN	TYP†	MAX	
V_{OH}	High-level output voltage*	I_{OH} = –400 μA	2.4			V
V_{OL}	Low-level output voltage*	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 5.25 V			10	μA
I_O	Output current (leakage)	V_O = 5.25 V			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V PD/$\overline{PGM}$ = V_{IL}			18	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		15	30	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

† Typical values are at T_A = 25°C and nominal voltages.

* AC and DC tests are made at 10% and 90% points using a 50% pattern.

capacitance over recommended supply voltage and operating free-air temperature range f = 1 MHz*

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† All typical values are T_A = 25°C and nominal voltage.

* This parameter is tested on sample basis only.

switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns See Figure 1		280	450	ns
$t_{a(S)}$	Access time from $\overline{CS}1$ and $\overline{CS}2$ (whichever occurs last)				120	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$			280	450	ns
$t_{v(A)}$	Output data valid after address change		0			ns
$t_{dis(S)}$	Output disable time from chip select during read only (whichever occurs last) ‡		0		100	ns
$t_{dis(PR)}$	Output disable time from PD/$\overline{PGM}$ during standby ‡		0		100	ns

† All typical values are at T_A = 25°C and nominal voltages.
‡ Value calculated from 0.5 volt delta to measured output level.

recommended timing requirements for programming T_A = 25°C (see note 4)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	0			ns

† Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming. AC and DC timing measurements are made at 90% points using a 50% pattern.
5. Common test conditions apply for t_{dis} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{dis}, PD/$\overline{PGM}$ = V_{IL}.

PARAMETER MEASUREMENT INFORMATION

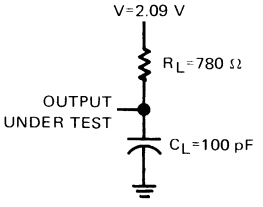

FIGURE 1 – TYPICAL OUTPUT LOAD CIRCUIT

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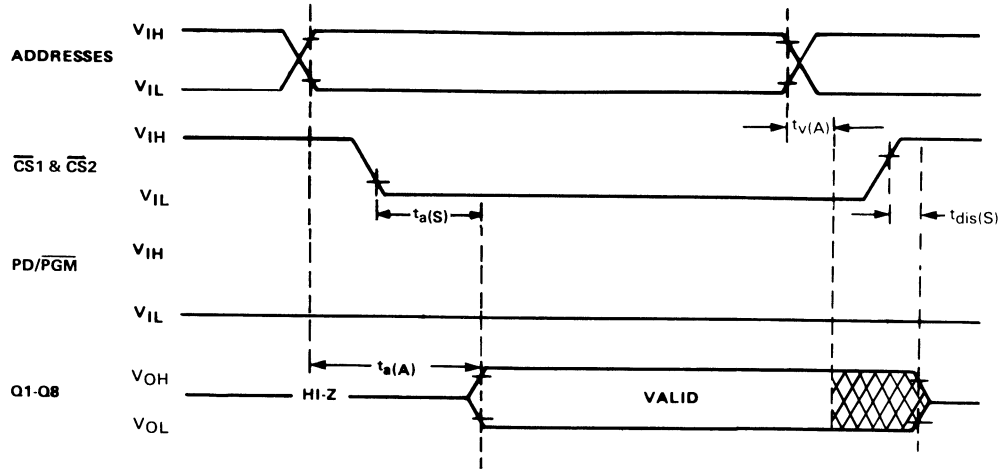
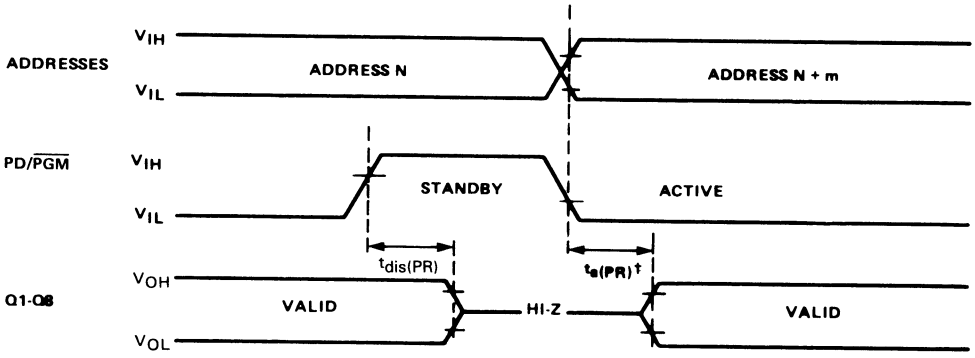
read cycle timing

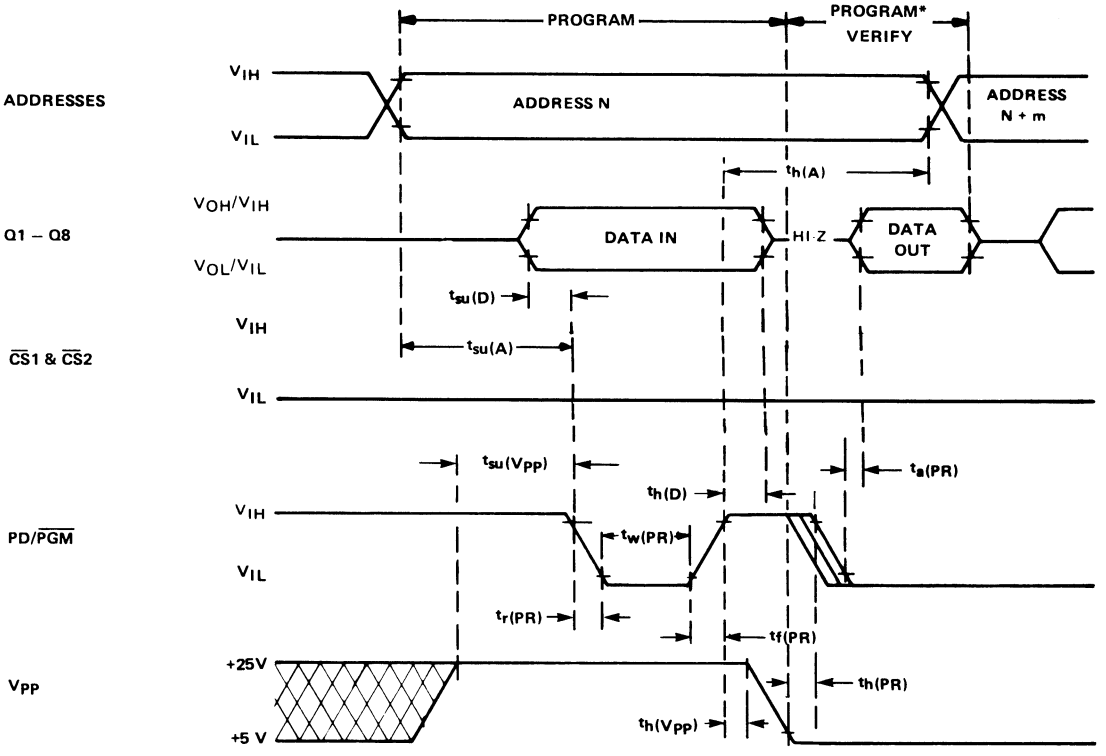


standby mode



† $t_{a(PR)}$ referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.
$\overline{CS1}$ and $\overline{CS2}$ in Don't Care State in Standby Mode.

program cycle timing



* Equivalent to read mode.

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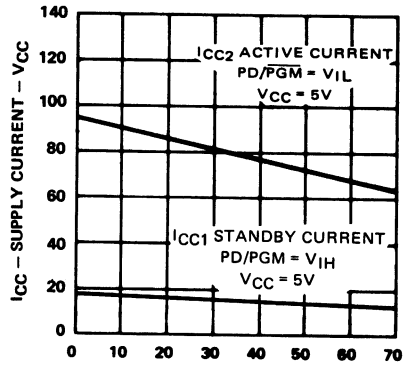
typical device characteristics (read mode)

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE



ACCESS TIME
vs
FREE-AIR TEMPERATURE