Micro Power Systems

# MP7574

CMOS
Microprocessor Compatible 8-Bit
Analog-to-Digital Converter

## FEATURES

- 8-Bit Resolution
- Fast Conversion Time: 20μs
- Interfaces to RAM, ROM or Slow-Memory
- Low Power Dissipation: 30mW
- Ratiometric Capability
- Single +5 V Supply Operation
- Internal Comparator
- Internal or External Clock Oscillator Operation

## BENEFITS

- Monolithic Reliability
- PDIP, CDIP and SOIC Packages Available

## APPLICATIONS

- Avionics
- Instrumentation
- Process Automation

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## GENERAL DESCRIPTION

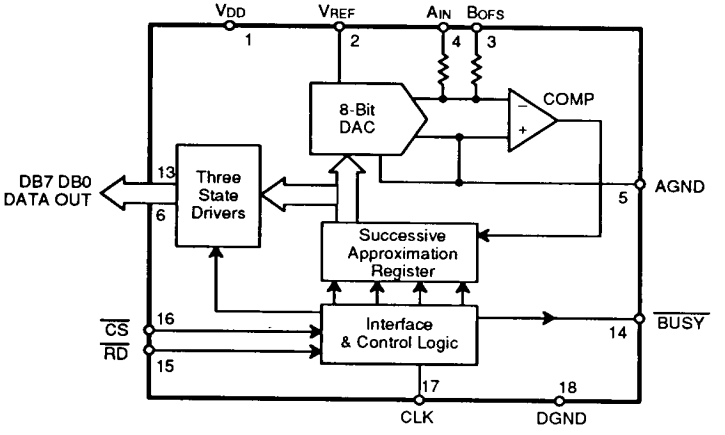
MP7574 is a low-cost, 8-bit μP compatible Analog-to-Digital Converter which uses a successive approximation technique to provide a maximum conversion time of 20μs.

Designed to operate as a memory mapped input device, the MP7574 can be interfaced like a static RAM, ROM, or slow-memory. The $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ/WRITE}$ control) inputs are available in all μP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the μP data bus or system input port.

Internal clock, +5 V operation, on-board comparator and interface logic, low power dissipation (30 mW) and fast conversion time make the MP7574 ideal for most ADC/μP interface applications. Small size (18-pin DIP) and monolithic reliability find wide use in avionics, instrumentation, and process automation applications.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7574 is available in Plastic and Ceramic dual-in-line, and Surface Mount (SOIC) packages.

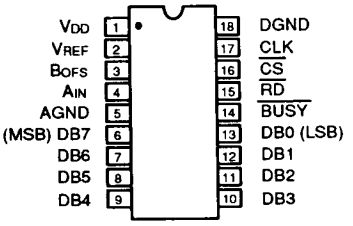
## SIMPLIFIED BLOCK DIAGRAM



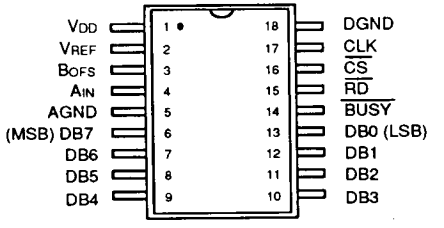
## ORDERING INFORMATION

| Package Type | Temperature Range | Part No. | INL (± LSB's) | DNL (± LSB's) |
|---|---|---|---|---|
| Plastic Dip | –40 to +85°C | MP7574JN | 3/4 | 7/8 |
| Plastic Dip | –40 to +85°C | MP7574KN | 1/2 | 3/4 |
| SOIC | –40 to +85°C | MP7574JS | 3/4 | 7/8 |
| SOIC | –40 to +85°C | MP7574KS | 1/2 | 3/4 |
| Ceramic Dip | –40 to +85°C | MP7574AD | 3/4 | 7/8 |
| Ceramic Dip | –40 to +85°C | MP7574BD | 1/2 | 3/4 |
| Ceramic Dip | –55 to +125°C | MP7574SD | 3/4 | 7/8 |
| Ceramic Dip | –55 to +125°C | MP7574SD/883 | 3/4 | 7/8 |
| Ceramic Dip | –55 to +125°C | MP7574TD | 1/2 | 3/4 |
| Ceramic Dip | –55 to +125°C | MP7574TD/883 | 1/2 | 3/4 |

## PIN CONFIGURATIONS




18 Pin PDIP, CDIP (0.300")




18 Pin SOIC (Jedec, 0.300")

## PIN OUT DEFINITIONS

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | $V_{DD}$ | +5 V Supply |
| 2 | $V_{REF}$ | –10 V Reference Input |
| 3 | $B_{OFS}$ | Bipolar Offset Input |
| 4 | $A_{IN}$ | Analog Input |
| 5 | AGND | Analog Ground |
| 6 | DB7 | Data Output Bit 7 (MSB) |
| 7 | DB6 | Data Output Bit 6 |
| 8 | DB5 | Data Output Bit 5 |
| 9 | DB4 | Data Output Bit 4 |

| PIN NO. | NAME | DESCRIPTION |
|---|---|---|
| 10 | DB3 | Data Output Bit 3 |
| 11 | DB2 | Data Output Bit 2 |
| 12 | DB1 | Data Output Bit 1 |
| 13 | DB0 | Data Output Bit 0 (LSB) |
| 14 | $\overline{BUSY}$ | Busy Output |
| 15 | $\overline{RD}$ | Read Input |
| 16 | $\overline{CS}$ | Chip Select Input |
| 17 | CLK | Clock Input |
| 18 | DGND | Digital Ground |

## ELECTRICAL CHARACTERISTICS TABLE

**Unless Otherwise Specified: $V_{DD}$ = +5 V, $V_{REF}$ = −10 V, Unipolar Configuration, $R_{CLK}$ = 180kΩ, $C_{CLK}$ = 100 pF**

| Parameter | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|---|
| **KEY FEATURES** | | | | | | | | |
| Resolution | | 8 | | | 8 | | Bits | |
| Sampling Rate | Fs | | | 50 | | 50 | kHz | |
| **ACCURACY (J, A, S Grades) (1)** | | | | | | | | |
| Differential Non-Linearity | DNL | | | ±7/8 | | ±7/8 | LSB | |
| Integral Non-Linearity | INL | | | ±3/4 | | ±3/4 | LSB | Best Straight Line |
| Full Scale Error (2) | EFS | | | ±5 | | ±6.5 | LSB | |
| Offset Error | | | | ±60 | | ±80 | mV | |
| **ACCURACY (K, B, T Grades) (1)** | | | | | | | | |
| Differential Non-Linearity | DNL | | | ±3/4 | | ±3/4 | LSB | |
| Integral Non-Linearity | INL | | | ±1/2 | | ±1/2 | LSB | Best Straight Line |
| Full Scale Error (2) | EFS | | | ±3 | | ±4.5 | LSB | |
| Offset Error | | | | ±30 | | ±50 | mV | |
| Mismatch between $B_{OFS}$ (pin 3) and $A_{IN}$ (pin 4) Resistances | | | | ±1.5 | | ±1.5 | % | |
| **ANALOG INPUT** | | | | | | | | |
| Input Resistance | | | | | | | | |
| at $V_{REF}$ (pin 2) | | 5 | 10 | 15 | 5 | 15 | kΩ | |
| at $B_{OFS}$ (pin 3) | | 10 | 20 | 30 | 10 | 30 | kΩ | |
| at $A_{IN}$ (pin 4) | | 10 | 20 | 30 | 10 | 30 | kΩ | |
| $V_{REF}$ (for specified performance) | | −10 | | | −10 | | V | |
| $V_{REF}$ Range | | −5 | | −15 | −5 | −15 | V | |
| Nominal Analog Input Range | | | | | | | | |
| Unipolar Mode | | 0 | | $V_{REF}$ | | | V | |
| Bipolar Mode | | $-\lvert V_{REF}\rvert$ | | $+\lvert V_{REF}\rvert$ | | | V | |
| **LOGIC INPUTS** | | | | | | | | |
| $\overline{RD}$ (pin 15), CS (pin 16) | | | | | | | | |
| $V_{INH}$ Logic HIGH Input Voltage | | 3.0 | | | 3.0 | | V | |
| $V_{INL}$ Logic LOW Input Voltage | | | | 0.8 | | 0.8 | V | |
| $I_{IN}$ Input Current | | | | ±1 | | ±10 | µA | $V_{IN}$ = 0 V, $V_{DD}$ |
| $C_{IN}$ Input Capacitance (3) | | | | 5 | | 5 | pF | |
| CLK (pin 17) | | | | | | | | |
| $V_{INH}$ Logic HIGH Input Voltage | | 3.0 | | | 3.0 | | V | |
| $V_{INL}$ Logic LOW Input Voltage | | | | 0.4 | | 0.8 | V | |
| $I_{INH}$ Logic HIGH Input Current | | | | 2 | | 3 | mA | During Conversion: $V_{IN}$ (CLK) ≥ $V_{INH}$(CLK) |
| $I_{INL}$ Logic LOW Input Current | | | | ±1 | | ±10 | µA | During Conversion: $V_{IN}$ (CLK) ≤ $V_{IN}$ (CLK) (See circuit of *Figure 8.* if external clock operation is required) |

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## ELECTRICAL CHARACTERISTICS TABLE (CONT'D)

| Description | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| **LOGIC OUTPUTS** | | | | | | | | |
| BUSY (pin 14), DB7 to DB0 (pins 6-13) | | | | | | | | |
| $V_{OH}$ Output HIGH Voltage | | 4.0 | | | 4.0 | | V | $I_{SOURCE}$ = 40µA |
| $V_{OL}$ Output LOW Voltage | | | 0.4 | 0.8 | | 0.8 | V | $I_{SINK}$ = 1.6mA |
| $I_{LKG}$ DB7 to DB0 Floating Stage Leakage | | | | 1 | | 10 | µA | $V_{OUT}$ = 0 V or $V_{DD}$ |
| Floating State Output Capacitance (3) (DB7 to DB0) | | | | 7 | | 7 | pF | |
| **POWER SUPPLIES** | | | | | | | | |
| $V_{DD}$ | | 4.75 | | 5.25 | 4.75 | 5.25 | V | 5V ±5% for specified performance |
| $I_{SS}$ (STANDBY) | | | | 5 | | 5 | mA | $A_{IN}$ = 0 V, ADC in RESET condition |
| $I_{REF}$ | | | | $V_{REF}/5k\Omega$ | | $V_{REF}/5k\Omega$ | | Conversion complete, prior to RESET |
| **AC PARAMETERS (3)** | | | | | | | | |
| **STATIC RAM INTERFACE MODE (See *Figure 1. and Table 1.*)** | | | | | | | | |
| $\overline{CS}$ Pulse Width Requirement | $t_{CS}$ | 100 | | | 150 | | ns | |
| $\overline{RD}$ to $\overline{CS}$ Setup Time | $t_{WSCS}$ | 0 | | | 0 | | ns | |
| $\overline{CS}$ to $\overline{BUSY}$ Propagation Delay | $t_{CBPD}$ | | 90 | 120 | | 180 | ns | $\overline{BUSY}$ Load = 20 pF |
| | | | 120 | 150 | | 200 | ns | $\overline{BUSY}$ Load = 100pF |
| $\overline{BUSY}$ to $\overline{RD}$ Setup Time | $t_{BSR}$ | 0 | | | 0 | | ns | |
| $\overline{BUSY}$ to $\overline{CS}$ Setup Time | $t_{BSCS}$ | 0 | | | 0 | | ns | |
| Data Access Time | $t_{RAD}$ | | 200 | 250 | 180 | 280 | ns | DB0-DB7 Load = 20pF |
| | | | 240 | 300 | | 400 | ns | DB0-DB7 Load = 100pF |
| Data Hold Time | $t_{RHD}$ | 50 | 80 | 120 | 30 | 180 | ns | |
| $\overline{CS}$ to $\overline{RD}$ Hold Time | $t_{RHCS}$ | | | 250 | | 500 | ns | |
| Reset Time Requirement | $t_{RESET}$ | 3 | | | 3 | | µs | |
| Conversion Time using internal clock oscillator | $t_{CONVERT}$ | | | | | | | See typical data of *Figure 5.* |
| Conversion Time using external clock | $t_{CONVERT}$ | | | 20 | | 20 | µs | $t_{CLK}$=400kHz |
| **ROM INTERFACE MODE (See *Figure 2.* and *Table 2.*)** | | | | | | | | |
| Data Access Time | $t_{RAD}$ | | | 250 | | 280 | | DB7-DB0, Load = 20pF |
| Data Hold Time | $t_{RHD}$ | | | 120 | | 180 | | DB7-DB0, Load = 100pF |
| RD HIGH to $\overline{BUSY}$ | $t_{WBPD}$ | | 0.4 | 1.5 | 0.3 | 2.0 | µs | $\overline{BUSY}$ Load = 20pF |
| Propagation Delay | $t_{WBPD}$ | | | 1.5 | 1.0 | 2.0 | µs | $\overline{BUSY}$ Load = 20 pF |
| $\overline{BUSY}$ to $\overline{RD}$ LOW Setup Time | $t_{BSR}$ | | | | | | | $\overline{RD}$ can go LOW prior to $\overline{BUSY}$ = HIGH, but must not return HIGH until $\overline{BUSY}$ = HIGH. *See Table 2.* |
| Conversion Time using internal clock oscillator | $t_{CONVERT}$ | | | | | | | See typical data of *Figure 5.* Add 2µs to data shown in *Figure 6.* for ROM Mode |

## ELECTRICAL CHARACTERISTICS TABLE

| Description | Symbol | 25°C Min | 25°C Typ | 25°C Max | Tmin to Tmax Min | Tmin to Tmax Max | Units | Conditions |
|---|---|---|---|---|---|---|---|---|
| **SLOW MEMORY INTERFACE MODE (See *Figure 3.* and *Table 3.*)** | | | | | | | | |
| $\overline{CS}$ to $\overline{BUSY}$ Propagation Delay | $t_{CBPD}$ | | | 120 | | 180 | ns | |
| Reset Time Requirement | $t_{RESET}$ | 3 | | | 3 | | µs | |
| Data Access Time | $t_{RAD}$ | | | 250 | | 280 | ns | Same as RAM Mode |
| Data Hold Time | $t_{RHD}$ | 50 | | 120 | 30 | 180 | ns | Same as RAM Mode |
| Conversion Time | $t_{CONVERT}$ | | | 20 | | 20 | µs | Same as RAM Mode |

**NOTES**
(1) Accuracy specifications are measured using the internal clock.
(2) Full scale error is measured after offset calibration.
(3) Guaranteed, not tested.

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**Specifications are subject to change without notice**

## ABSOLUTE MAXIMUM RATINGS (1, 2) ($T_A$ = +25°C unless otherwise noted)

$V_{DD}$ to AGND ..... 0 V, +7.0 V
$V_{DD}$ to DGND ..... 0 V, +7.0 V
AGND to DGND ..... GND –0.5 to $V_{DD}$ +0.5 V
Digital Input Voltage to DGND
(pins 15 and 16) ..... –0.5 V to +15 V
Digital Output Voltage to DGND
(pins 6–14) ..... GND –0.5 to $V_{DD}$ +0.5 V
CLK Input Voltage to DGND
(pin 17) ..... GND –0.5 to $V_{DD}$ +0.5 V
$V_{REF}$ (pin 2) ..... ±20 V
$V_{BOFS}$ (pin 3) ..... ±20 V
$V_{AIN}$ (pin 4) ..... ±20 V
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature (soldering, 10 secs) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP ..... 450mW
Derates above 75°C ..... 6mW/°C
Package Power Dissipation Rating to 70°C
PDIP, SOIC ..... 670mW
Derates above 75°C ..... 8.3mW/°C

**NOTES:**
(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies.

## TIMING AND CONTROL OF THE MP7574

### Static RAM Interface Mode

*Table 1.* and *Figure 1.* show the truth table and timing requirements for MP7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the MP7574 (once a conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the MP7574 address location.

$\overline{BUSY}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the MP7574 conversion time. The delay can be generated by inserting NOP instructions (or other program instructions) between the WRITE (start convert) and READ (read data) operations. Once $\overline{BUSY}$ is HIGH (conversion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the MP7574. The data is lost when $\overline{RD}$ returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ and a convert start.

| MP7574 Inputs | | MP7574 Outputs | | MP7574 Operation |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{RD}$ | $\overline{BUSY}$ | DB7-DB0 | |
| L | H | H | High Z | Write Cycle (Start Convert) |
| L | ↓ | H | High Z→Data | Read cycle (Data Read) |
| L | ↑ | H | Data→High Z | Reset Converter |
| H | X[1] | X | High Z | Not selected |
| L | H | L | High Z | No effect, converter busy |
| L | ↓ | L | High Z | No effect, converter busy |
| L | ↑ | L | High Z | Not allowed, causes incorrect conversion |

NOTE 1: If $\overline{RD}$ goes LOW to HIGH when $\overline{CS}$ is LOW, the ADC is internally reset, $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH. See Application Hint Number 1.

**Table 1. Truth Table, Static RAM Mode**

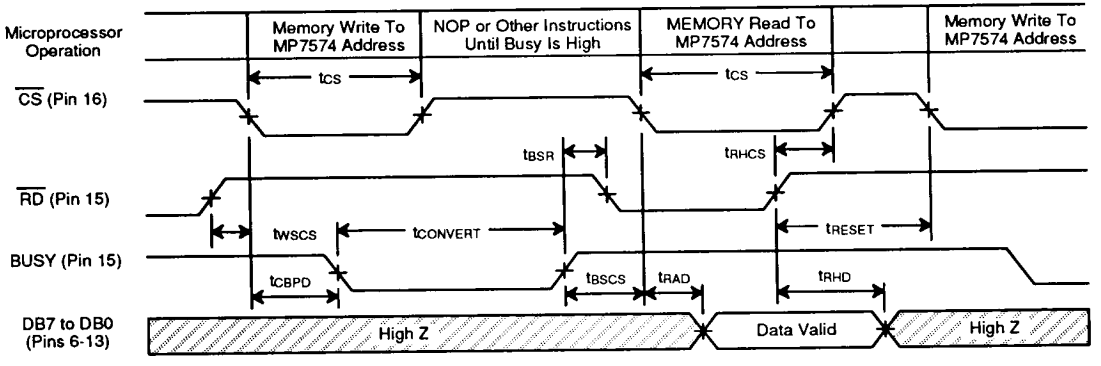


**Figure 1. Static RAM Mode Timing Diagram**

## ROM Interface Mode

*Table 2.* and *Figure 2.* show the truth table and timing requirements for interfacing the MP7574 as a Read Only Memory.

$\overline{CS}$ is held LOW and converter operation is controlled by the $\overline{RD}$ input. The MP7574 $\overline{RD}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the MP7574 address location. The converter is automatically restarted when $\overline{RD}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{BUSY}$ is HIGH will result in incorrect output data.

| MP7574 Inputs | | MP7574 Outputs | | MP7574 Operation |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{RD}$ | $\overline{BUSY}$ | DB7-DB0 | |
| L | ⊓ | H | High Z→Data | Data Read |
| L | ⊔ | ⊓ | Data→High Z | Reset and start new conversion |
| L | ⊓ | L | High Z | No effect, converter busy |
| L | ⊔ | L | High Z | Not allowed, causes incorrect conversion |

**Table 2. Truth Table, Static ROM Mode**

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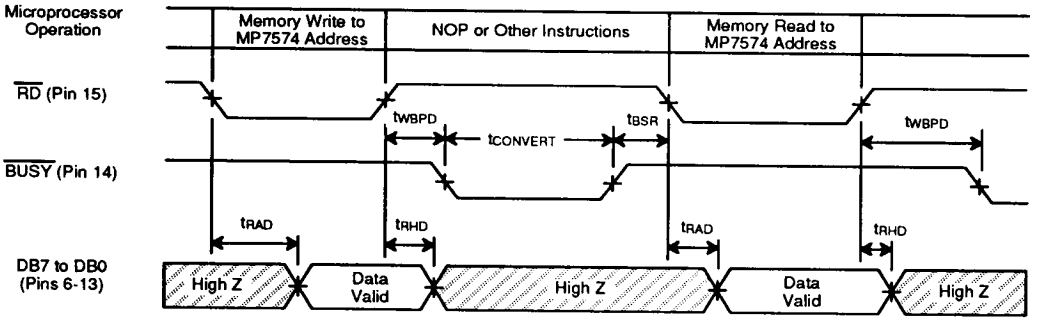


**Figure 2. ROM Mode Timing Diagram ($\overline{CS}$ Held Low)**

## Slow-Memory Interface Mode

*Table 3.* and *Figure 3.* show the truth table and timing requirements for interfacing the MP7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{CS}$ and $\overline{RD}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the MP7574 $\overline{CS}$ and $\overline{RD}$ inputs. $\overline{BUSY}$ is connected to the microprocessor READY input.

When the MP7574 is NOT addressed, the $\overline{CS}$ and $\overline{RD}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the MP7574 address. $\overline{BUSY}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{BUSY}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

| MP7574 Inputs | MP7574 Outputs | | MP7574 Operation |
|---|---|---|---|
| $\overline{CS}$ & $\overline{RD}$ | $\overline{BUSY}$ | DB7-DB0 | |
| H | H | High Z | Not selected |
| ⌐ | ⌐ | High Z | Start conversion |
| L | L | High Z | Conversion in progress, µP in wait state |
| L | ⌐ | High Z→Data | Conversion Complete, µP reads data |
| ⌐ | H | Data→High Z | Converter reset and deselected |
| H | H | High Z | Not selected |

**Table 3. Truth Table, Slow Memory Mode**

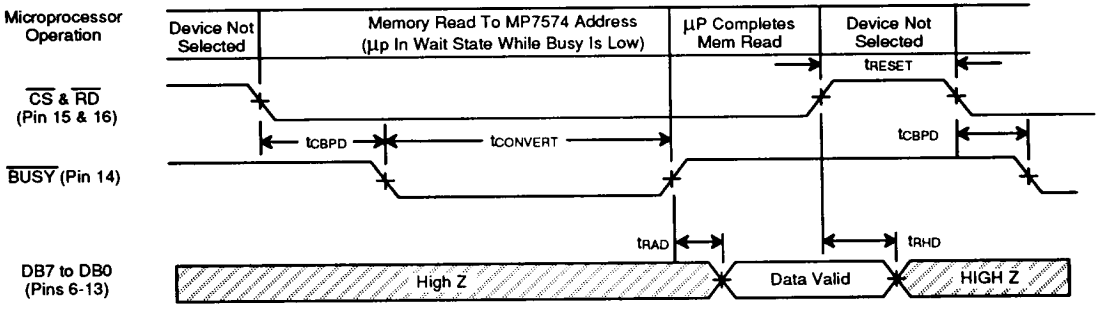


**Figure 3. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)**

## GENERAL CIRCUIT INFORMATION

### Basic Circuit Description

The MP7574 uses a successive approximation technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a −10 V reference, and a +5 V supply.

*Figure 4.* shows the MP7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins for Control Logic and Timing Details, $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB), are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, AIN. If the sum of the DAC bits is less than AIN, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than AIN, the trial bit is turned OFF and the next smaller bit it tried.

Each successively smaller bit is tried and compared to AIN in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the DB0 - DB7 data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

### DAC Circuit Details

The current weighted D/A converter is a precision multiplying DAC. *Figure 4.* shows the functional diagram of the DAC as used in the MP7574. It consists of a precision thin film R/2R ladder network and 8 N-Channel MOSFET switches operated as single-pole-double-throw switches.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is $V_{REF}$ divided by 2R, in the second arm is $V_{REF}$ divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arm is steered either to AGND or to the comparator summing point.

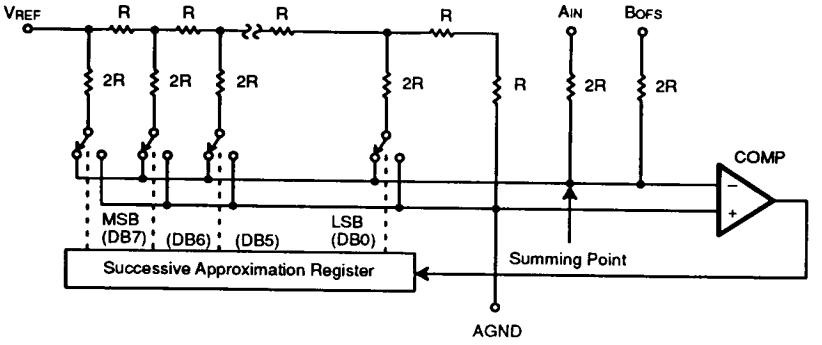


**Figure 4. D/A Converter as Used in MP7574**

## OPERATING THE MP7574

### Application Hints

1. Timing & Control: In the MP7574 when a conversion is finished the fresh data must be read before a new conversion can be started. Failure to observe the timing restrictions of *Figures 1, 2 or 3* may cause the MP7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).

2. Logic Deglitching In µP Applications: Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the MP7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert start, read, or reset. The best way to avoid glitches is to gate the address decoding logic with $\overline{RD}$ or $\overline{WR}$ (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow–memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.

3. Input Loading at $V_{REF}$, $A_{IN}$ and $B_{OFS}$: To prevent loading errors due to the finite input resistance at the $V_{REF}$, $A_{IN}$ or $B_{OFS}$ pins, low impedance driving sources must be used (i.e. op amp buffers or low output – Z reference).

4. Ratiometric Operation: Ratiometric performance is inherent in A/D converters such as the MP7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than –10 V in magnitude.

5. Offset Correction: Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the MP7574 $A_{IN}$ pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider between $V_{DD}$ and $V_{REF}$ and applying the tap voltage to the amplifier's positive input.

6. Analog and Digital Ground: It is recommended that AGND and DGND be connected locally to prevent the possibility of injecting noise into the MP7574. In systems where the AGND - DGND connection is not local, connect back-to-back diodes (IN914 or equivalent) between the MP7574 AGND and DGND pins.

7. Initialization After Power Up: Execute a memory READ to the MP7574 address location, and subsequently ignore the data. The MP7574 is internally reset when reading out data.

## CLOCK OSCILLATOR

The MP7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and stops when conversion is complete.

The clock oscillator requires an external R and C as shown in *Figure 5.* Nominal conversion time versus $R_{CLK}$ and $C_{CLK}$ is shown in *Figure 6.* The curves shown in *Figure 6.* are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2µs to the typical conversion time values shown.

The MP7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 20µs, as indicated by the unshaded region of *Figure 6.* Conversion times faster than 20µs can cause transfer accuracy degredation.

## OPERATION WITH EXTERNAL CLOCK

For applications requiring conversion time close to or equal to 15µs, an external clock is recommended. Using an external clock includes the possibility of converting faster than 15µs (which can cause transfer accuracy degradation) due to temperature drift - as may be the case when using the internal clock oscillator.

*Figure 7.* shows how the external clock must be connected. The $\overline{BUSY}$ output of the MP7574 is connected to the three-state enable input of a 74125 three-state buffer. R1 is used as a pullup, and can be between 6KΩ and 100KΩ. A 500kHz clock will provide a conversion time of 15µs.

The external memory clock should be used only in the static RAM or slow memory interface mode, and not in the ROM mode.

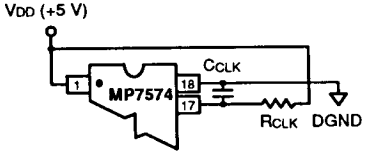


**Figure 5. Connecting RCLK and CCLK to CLK Oscillator**

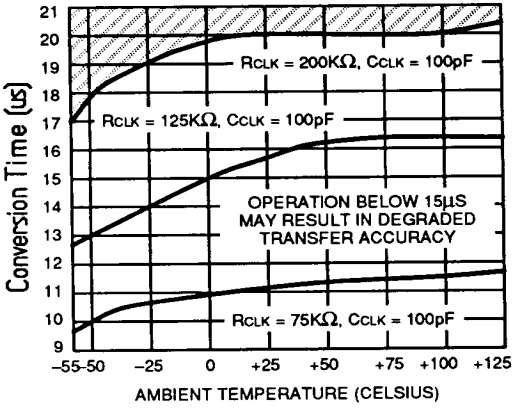


**Figure 6. Typical Conversion Time vs. Temperature for Different RCLK and CCLK (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2µs to values shown)**

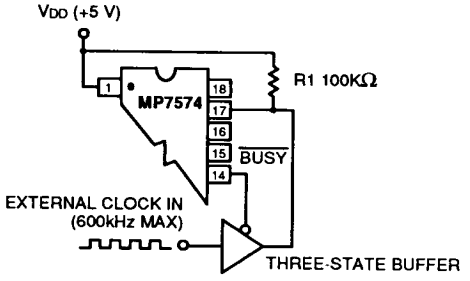


**Figure 7. External Clock Operation (Static RAM and Slow-Memory Mode)**

Timing constraints for external clock operation are as follows:

### Static RAM Mode

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after $\overline{BUSY}$ = 1.

### Slow Memory Mode

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

3

## UNIPOLAR BINARY OPERATON

*Figure 8. and Figure 9.* show the analog circuit connections and typical transfer characteristic for unipolar operation. A REF01 or REF02 is used as the –10 V reference.

Calibration is as follows:

OFFSET: Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminal.

1. Apply – 39.1 mW (1 LSB) to the input of the buffer amplifier used to drive R1 (i.e. +39.1 mW at R1).
2. While performing continuous conversions, adjust the offset potentiometer (described above) until DB7 - DB1 are LOW and the LSB (DB0) flickers.

Gain (Full Scale): Offset adjustment must be performed before gain adjustment.

1. Apply –9.961 V to the input of the buffer amplifier used to drive R1 (i.e. +9.961 V at R1).
2. While performing continuous conversions, adjust trim pot R2 until DB7 – DB1 are HIGH and the LSB (DB0) flickers.

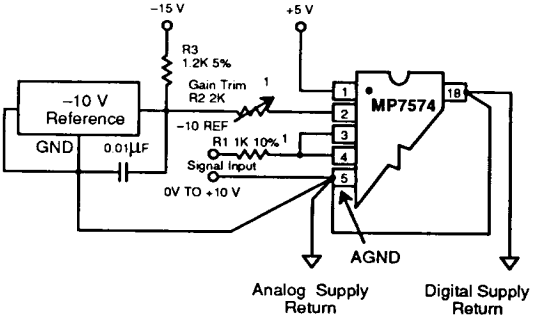


**Figure 8. MP7574 Unipolar (0 V to +10 V) Operation (Output Code is Straight Binary)**

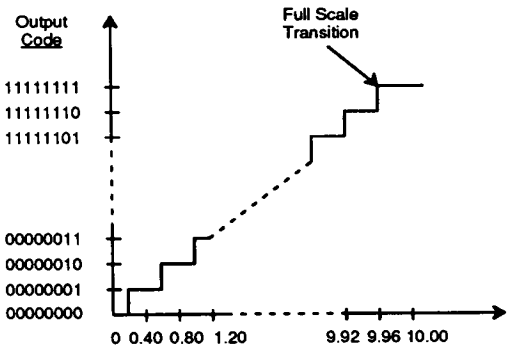


**Figure 9. Nominal Transfer Characteristic for Unipolar Circuit of Figure 8.**

7. Doing continuous conversions, trim R2 until DB7 – DB1 are LOW and the LSB (DB0) flickers.
8. Apply −9.92 V to the input of the buffer amplifier (i.e. +9.92 V at the input side of R6.)
9. If the ADC output code is not 11111110 +1 bit, repeat the calibration procedure.

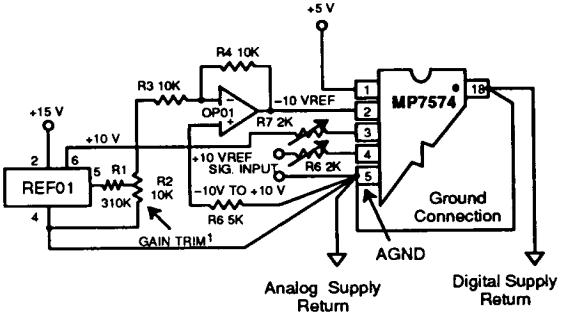


**Figure 10. MP7574 Bipolar (−10 V to +10 V) Operation (Output Code is Offset Binary)**

## Bipolar (Offset Binary) Operation

*Figure 10. and Figure 11.* illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of *Figure 10.* (resistors R8, R9 and R10 in *Figure 10.* show how offset trim can be done at the buffer amplifier.)

Calibration is as follows:

1. Adjust R6 and R7 for minimum resistance across the potentiometers.
2. Apply +10.000 V to the buffer amplifier used to drive the signal input (i.e. −10.000 V at R6).
3. While performing continuous conversions, trim R6 or R7 (whichever required) until DB7 – DB1 are LOW and the LSB (DB0) flickers.
4. Apply 0 V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000 V to the input of the buffer amplifier (i.e. −10.000 V as applied to R6.)

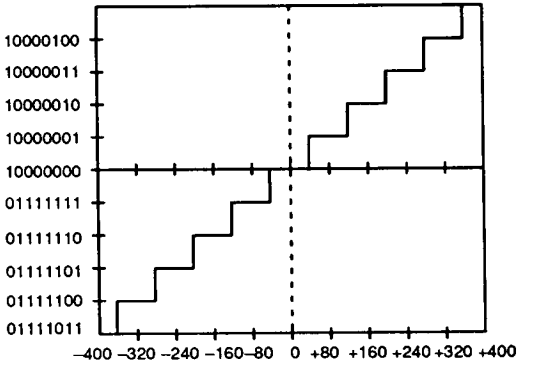


**Figure 11. Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10.**