8251A
PROGRAMMABLE COMMUNICATION INTERFACE

- Synchronous and Asynchronous Operation
- Synchronous 5–8 Bit Characters; Internal or External Character Synchronization; Automatic Sync Insertion
- Asynchronous 5–8 Bit Characters; Clock Rate—1, 16 or 64 Times Baud Rate; Break Character Generation; 1, 1½, or 2 Stop Bits; False Start Bit Detection; Automatic Break Detect and Handling
- Synchronous Baud Rate—DC to 64K Baud
- Asynchronous Baud Rate—DC to 19.2K Baud
- Full-Duplex, Double-Buffered Transmitter and Receiver
- Error Detection—Parity, Overrun and Framing
- Compatible with an Extended Range of Intel Microprocessors
- 28-Pin DIP Package
- All Inputs and Outputs are TTL Compatible
- Available in EXPRESS and Military Versions

The 8251A is the industry standard Universal Synchronous/Asynchronous Receiver/Transmitter (USART) designed for data communications with microprocessor families such as MCS-48, 80, 85, and iAPX 86, 88. The 8251A is used as a peripheral device and is programmed by the CPU to operate using virtually any serial data transmission technique presently in use (including IBM "bi-sync"). The USART accepts data characters from the CPU in parallel format and then converts them into a continuous serial data stream for transmission. Simultaneously, it can receive serial data streams and convert them into parallel data characters for the CPU. The USART will signal the CPU whenever it can accept a new character for transmission or whenever it has received a character for the CPU. The CPU can read the complete status of the USART at any time. These include data transmission errors and control signals such as SYNDET, TxEMPTY. The chip is fabricated using Intel's high performance HMOS technology.

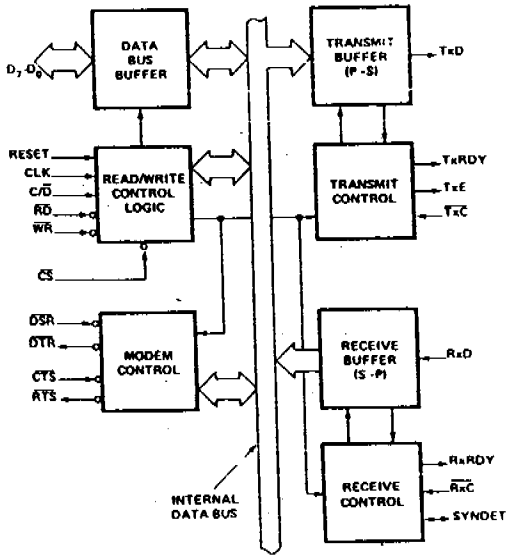


Figure 1. Block Diagram

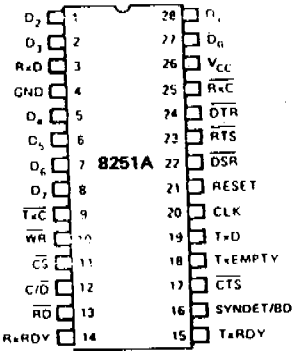


Figure 2. Pin Configuration

**** For complete Rochester ordering guide, please refer to page 2 ****

Rochester Ordering Guide

Rochester Part Number	OCM Part Number	Package	Temperature
D8251A	D8251A	DIP-28	0° to +70°C
ID8251A	ID8251A	DIP-28	-40° to +85°C
LD8251A	LD8251A	DIP-28	-40° to +85°C
P8251A	P8251A	DIP-28	0° to +70°C
QD8251A	QD8251A	DIP-28	0° to +70°C
QP8251A	QP8251A	DIP-28	0° to +70°C
TD8251A	TD8251A	DIP-28	-40° to +85°C

Operating Conditions

Symbol	Description	Min	Max	Units
TC	Case Temperature (Instant On)	0	+70	° C
VCC	Digital Supply Voltage	4.5	5.5	V

D.C. Characteristics (Over Specified Operating Conditions)

Symbol	Parameter	Min	Max	Unit	Comments
VIL	Input Low Voltage		0.8	V	
VIH	Input High Voltage	2.0		V	
VOL	Output Low Voltage		0.45	V	IOL = 2.2 mA
VOH	Output High Voltage	2.4		V	IOL = -400 µA
IOFL	Output Float Leakage		± 10	µA	VOUT = VCC to 0.45V
IIL	Input Leakage		± 10	µA	VIN = VCC to 0.45V
ICC	Power Supply Current		100	mA	(Note 9)

CAPACITANCE TC = 25°C; VCC = GND = 0V

Symbol	Parameter	Min	Max	Unit	Comments
CIN	Input Capacitance		10	pF	FC = 1 MHz
CI/O	I/O Capacitance		20	pF	Unmeasured Pins Returned to GND

A.C. Characteristics (Over Specified Operating Conditions)
Bus Parameters (Note 1)

Read Cycle

Symbol	Parameter	Min	Max	Unit	Comments
tAR	Address Stable Before READ (CS, C/D)	0		ns	(Note 2)
tRA	Address Hold Time for READ (CS, C/D)	0		ns	(Note 2)
tRR	READ Pulse Width	250		ns	
tRD	Data Delay form READ		200	ns	(Note 3)
tDF	READ ↑ to Data Floating	10	100	ns	

A.C Characteristics (Over Specified Operating Conditions)

Write Cycle

Symbol	Parameter	Min	Max	Unit	Comments
tAW	Address Stable Before WRITE	0		ns	
tWA	Address Hold Time for WRITE	20		ns	
tWW	WRITE Pulse Width	250		ns	
tDW	Data Set-Up Time for WRITE	150		ns	
tWD	Data Hold Time for WRITE	20		ns	

Other Timings

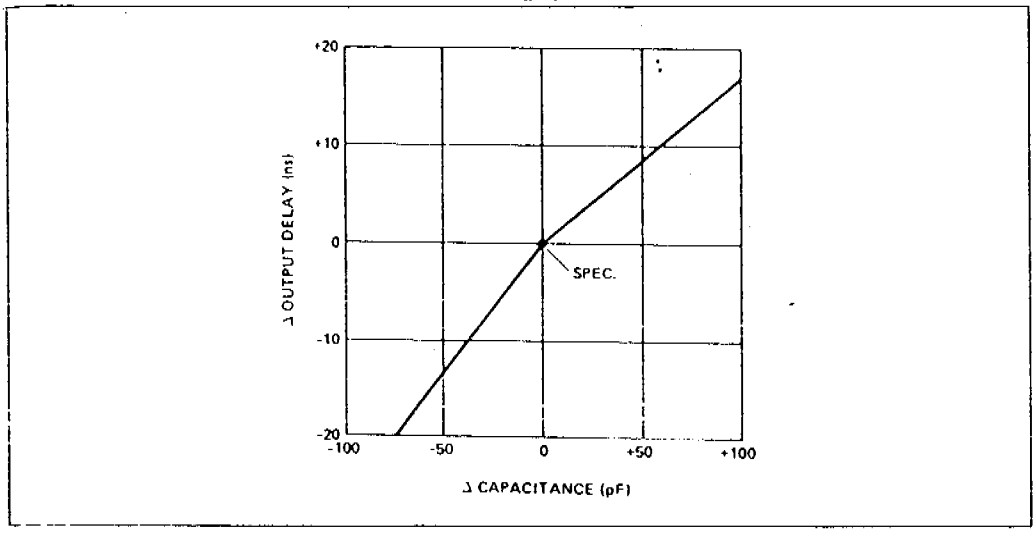
Symbol	Parameter	Min	Max	Unit	Comments
tCY	Clock Period	320	1350	ns	(Notes 4,5)
tø	Clock High Pulse Width	120	tCY -90	ns	
tø	Clock Low Pulse Width	90		ns	
tR, tF	Clock Rise and Fall Time		20	ns	
fTx	Transmitter Input Clock Frequency				
	1x Baud Rate	DC	64	KHz	
	16x Baud Rate	DC	310	KHz	
	64x Baud Rate	DC	615	KHz	
tTPW	Transmitter Input Clock Pulse Width				
	1x Baud Rate	12		tCY	
	16x and 64x Baud Rate	1		tCY	
tTPD	Transmitter Input Clock Pulse Delay				
	1x Baud Rate	15		tCY	
	16x and 64x Baud Rate	3		tCY	
fRx	Receiver Input Clock Frequency				
	1x Baud Rate	DC	64	KHz	
	16x Baud Rate	DC	310	KHz	
	64x Baud Rate	DC	615	KHz	
tRPW	Receiver Input Clock Pulse Width				
	1x Baud Rate	12		tCY	
	16x and 64x Baud Rate	1		tCY	
tRPD	Receiver Input Clock Pulse Delay				
	1x Baud Rate	15		tCY	
	16x and 64x Baud Rate	3		tCY	
tTxRDY	TxRDY Pin Delay from Center of Last Bit		14	tCY	(Note 6)
tTxRDY CLEAR	TxRDY ↓ from Leading Edge of WR		400	ns	(Note 6)
tRxRDY	RxRDY Pin Delay from Center of Last Bit		26	tCY	(Note 6)
tRxrdy CLEAR	RxRDY ↓ from Leading Edge of RD		400	ns	(Note 6)
tIS	Internal SYNDET Delay from Rising Edge of RxC		26	tCY	(Note 6)
tES	External SYNDET Set-Up Time After Rising Edge of RxC	16	(Note 7)	tCY	(Note 6,8)
tTxEMPTY	TxEMPTY Delay from Center of Last Bit		20	tCY	(Note 6)
tWC	Control Delay from Rising Edge of WRITE (TxEn, DTR, RTS)		8	tCY	(Note 6)
tCR	Control to READ Set-up Time (DSR, CTS)	20		tCY	(Note 6)

NOTES:

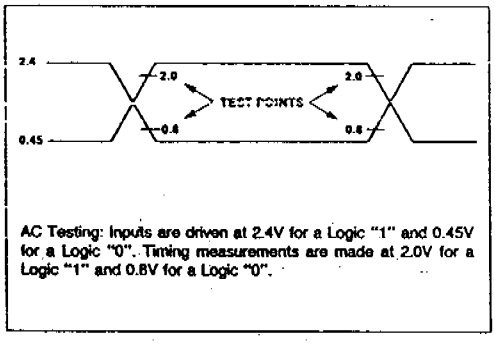
1. AC timings measured VOH = 2.0, VOL = 0.8.
2. Chip Select (CS) and Command/Data (C/D) are considered as Addresses.
3. Assumes that Address is valid before RD ↓.
4. The TxC and RxC frequencies have the following limitations with respect to CLK:
   For 1x Baud Rate, fTX or fRx ≤ 1/(30 tCY):
   For 16x and 64x Baud Rate, fTX or fRx ≤ 1/(4.5 tCY).
5. Reset Pulse Width = 6 tCY minimum; System Clock must be running during Reset.
6. Status update can have a maximum delay of 28 clock periods from the event affecting the status.
7. Before falling edge of RxC.
8. In external synch mode the tES spec. requires the ratio of the system clock (CLK) to receive or transmit bit ratios t greater than 34.
9. ICC is measured in a static condition with outputs in the worst condition with all outputs unloaded.

A.C. CHARACTERISTICS (Continued)

TYPICAL Δ OUTPUT DELAY VS. Δ CAPACITANCE (pF)



A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING LOAD CIRCUIT

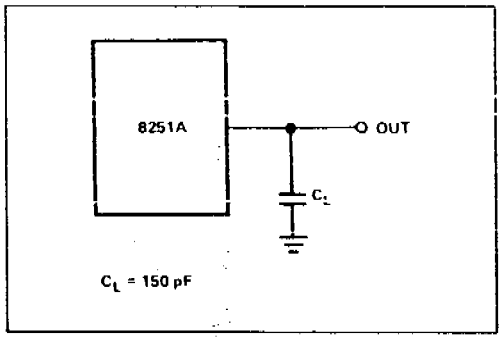
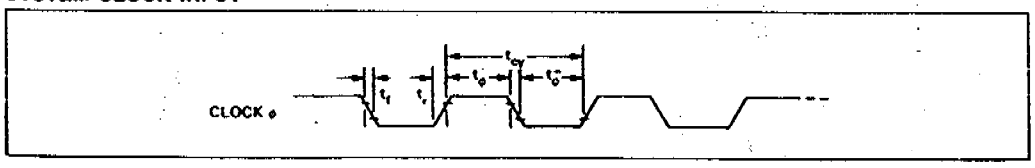


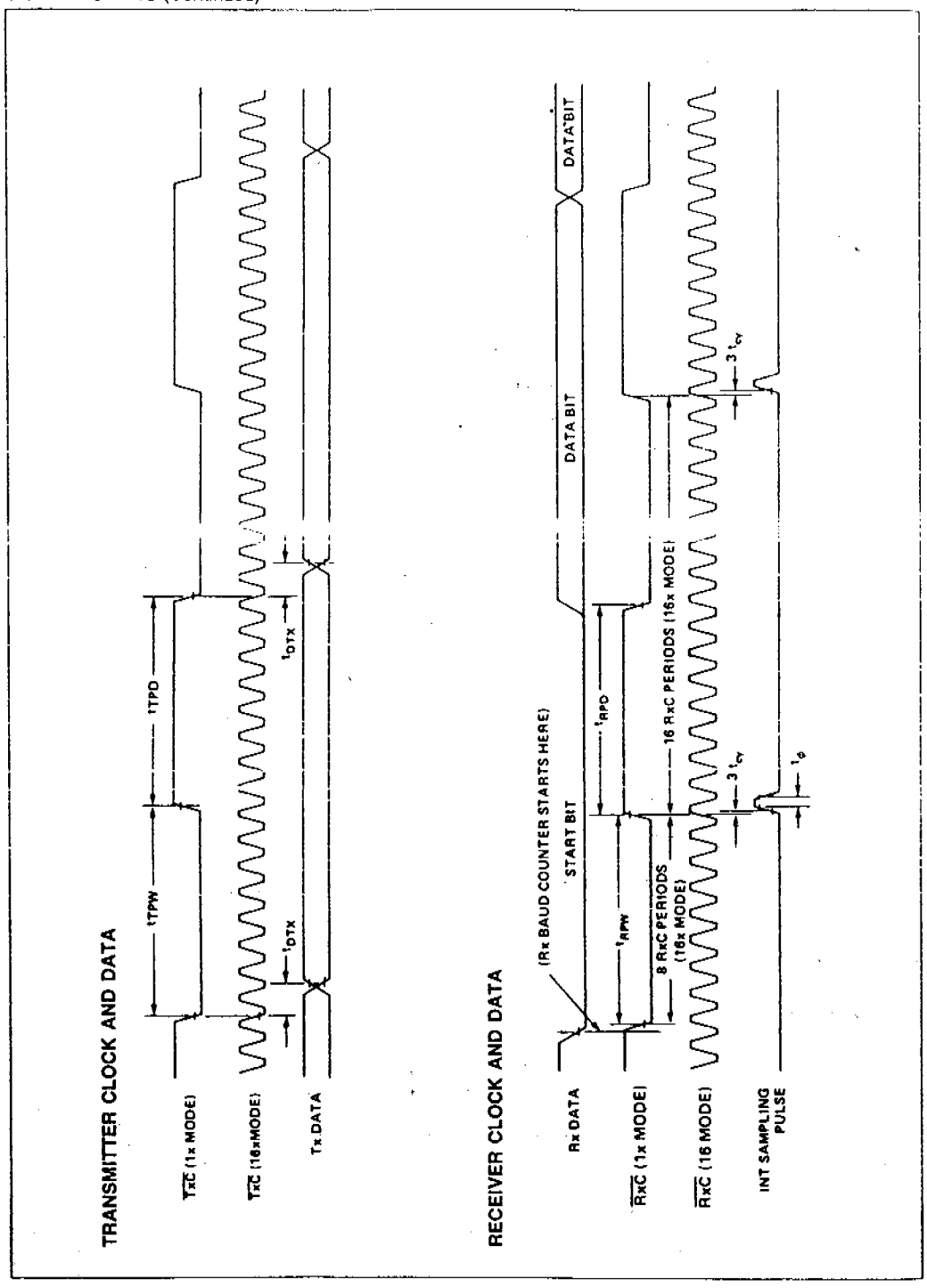
Figure 18

WAVEFORMS

SYSTEM CLOCK INPUT

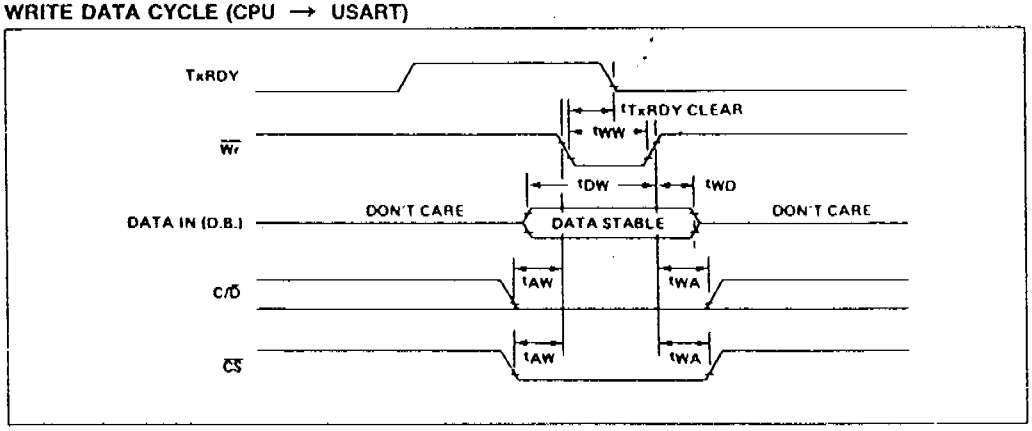


WAVEFORMS (Continued)

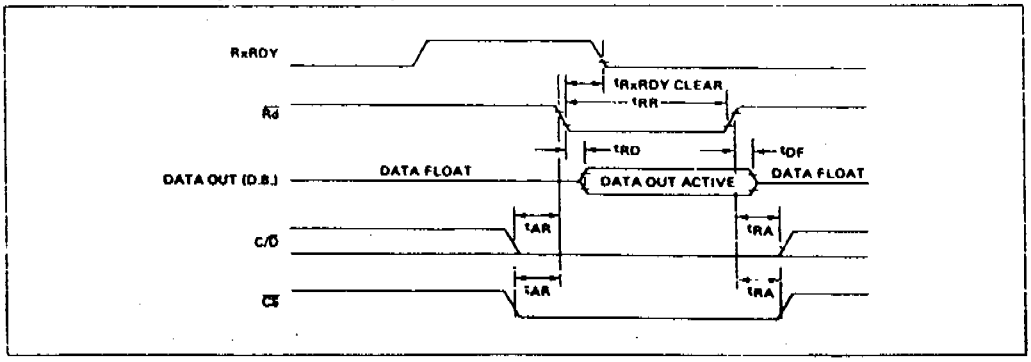


WAVEFORMS (Continued)

WRITE DATA CYCLE (CPU → USART)

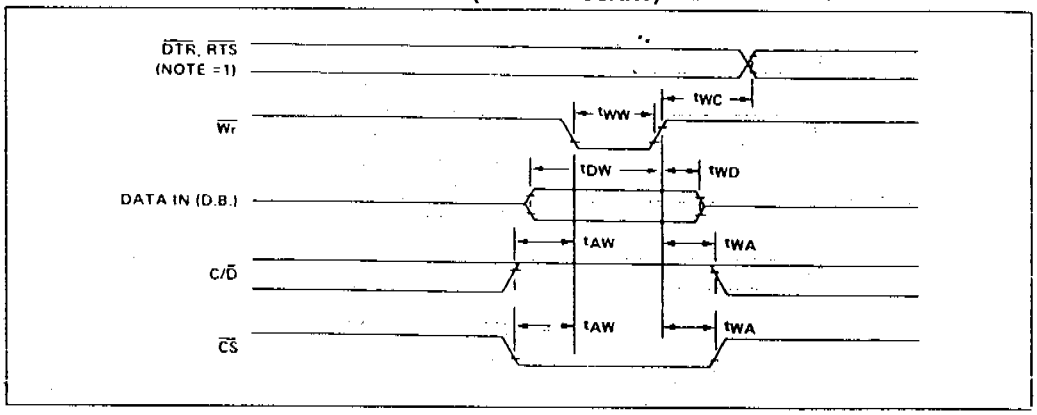


READ DATA CYCLE (CPU ← USART)

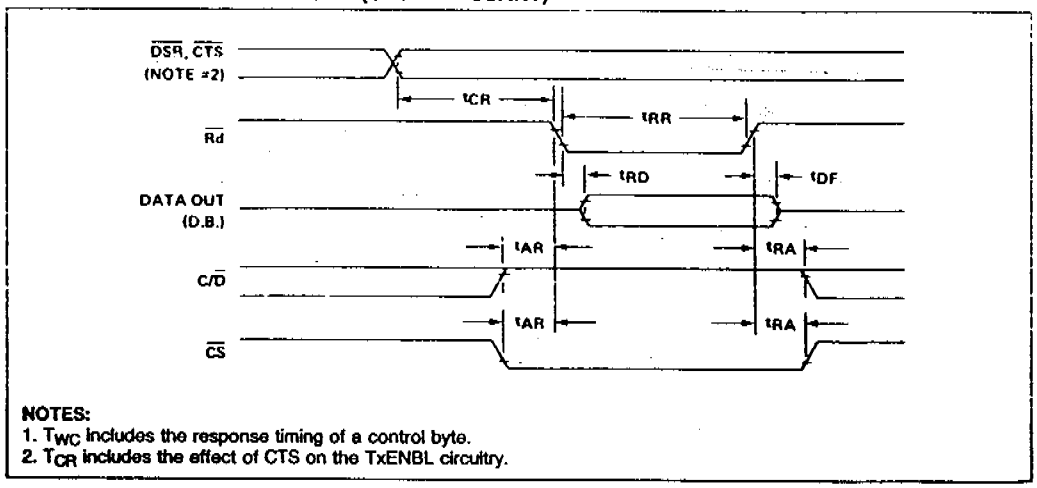


WAVEFORMS (Continued)

WRITE CONTROL OR OUTPUT PORT CYCLE (CPU → USART)

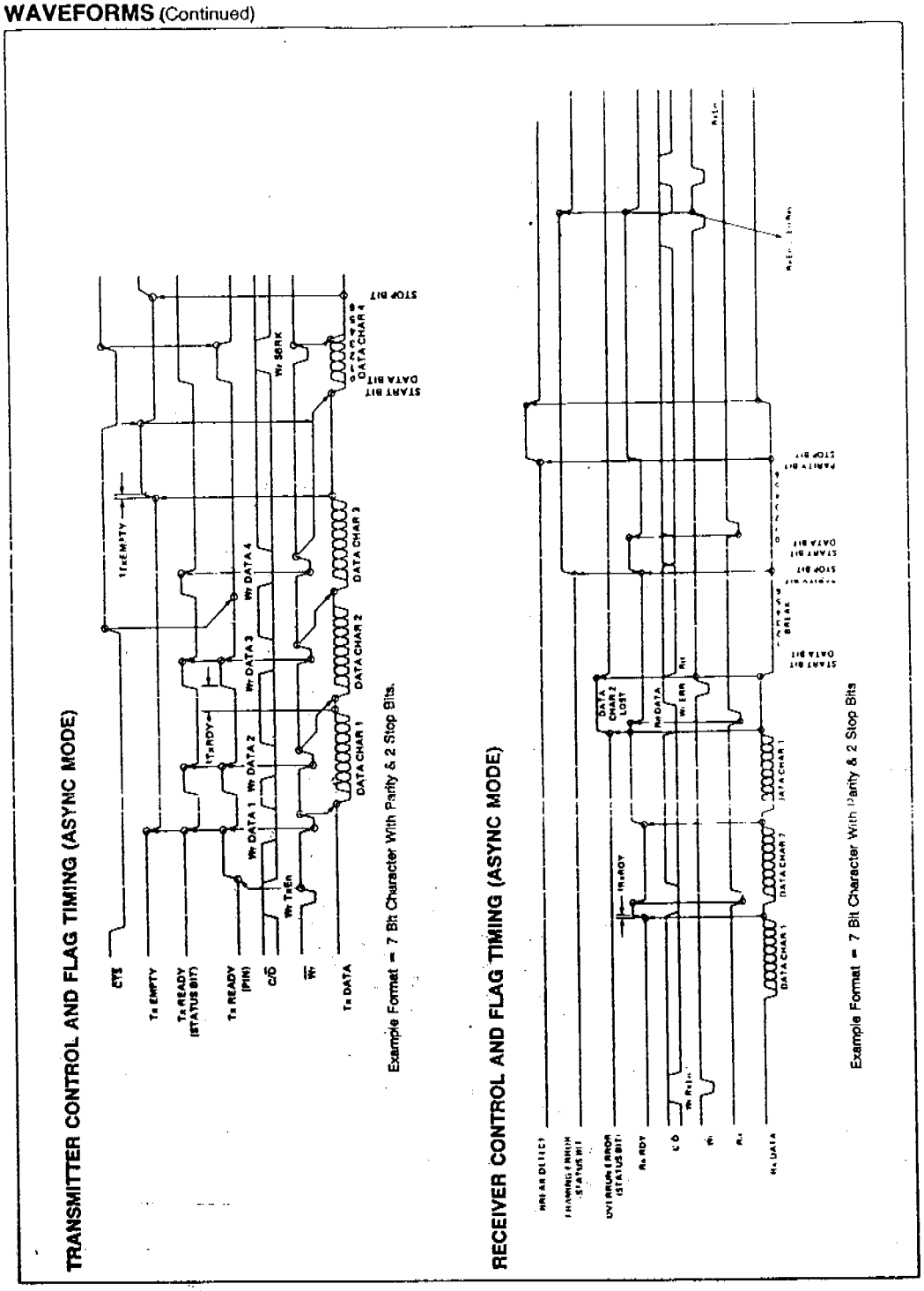


READ CONTROL OR INPUT PORT (CPU ← USART)



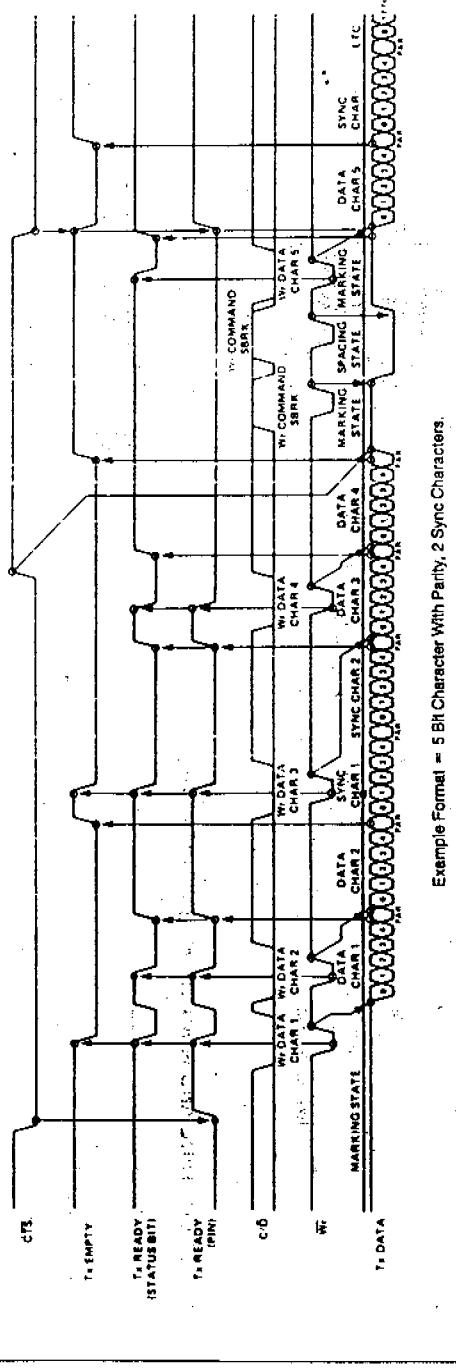
NOTES:
1. T_{WC} includes the response timing of a control byte.
2. T_{CR} includes the effect of CTS on the TxENBL circuitry.

WAVEFORMS (Continued)



WAVEFORMS (Continued)

TRANSMITTER CONTROL AND FLAG TIMING (SYNC MODE)



WAVEFORMS (Continued)