FAIRCHILD
A Schlumberger Company

μA2240 Programmable Timer/Counter

Linear Division Special Functions

Description

The μA2240 Programmable Timer/Counter is a monolithic controller capable of producing accurate microsecond to five day time delays. Long delays, up to three years, can easily be generated by cascading two timers. The timer consists of a time-base oscillator, programmable 8-bit counter and control flip-flop. An external resistor capacitor (RC) network sets the oscillator frequency and allows delay times from 1 RC to 255 RC to be selected. In the astable mode of operation, 255 frequencies or pulse patterns can be generated from a single RC network. These frequencies or pulse patterns can also easily be synchronized to an external signal. The trigger, reset and outputs are all TTL and DTL compatible for easy interface with digital systems. The timer's high accuracy and versatility in producing a wide range of time delays makes it ideal as a direct replacement for mechanical or electromechanical devices.

- **Accurate Timing From Microseconds To Days**
- **Programmable Delays From 1 RC To 255 RC**
- **TTL, DTL And CMOS Compatible Outputs**
- **Timing Directly Proportional To RC Time Constant**
- **High Accuracy**
- **External Sync And Modulation Capability**
- **Wide Supply Voltage Range**
- **Excellent Supply Voltage Rejection**

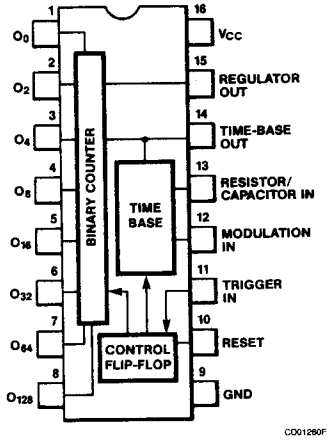
Absolute Maximum Ratings

Storage Temperature Range	
Ceramic DIP	−65°C to +175°C
Molded DIP	−65°C to +150°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Ceramic DIP (soldering, 60 s)	300°C
Molded DIP (soldering, 10 s)	265°C
Internal Power Dissipation[1, 2]	
16L-Ceramic DIP	1.50 W
16L-Molded DIP	1.04 W
Supply Voltage	18 V
Output Current	10 mA
Output Voltage	18 V
Regulator Output Current	5.0 mA

Notes

1. $T_{J\ Max}$ = 150°C for the Molded DIP, and 175°C for the Ceramic DIP.
2. Ratings apply to ambient temperature at 25°C. Above this temperature, derate the 16L-Ceramic DIP at 10 mW/°C, and the 16L-Molded DIP at 8.3 mW/°C.

Connection Diagram 16-Lead DIP (Top View)



CD01260F

Order Information

Device Code	Package Code	Package Description
μA2240DC	7B	Ceramic DIP
μA2240PC	9B	Molded DIP

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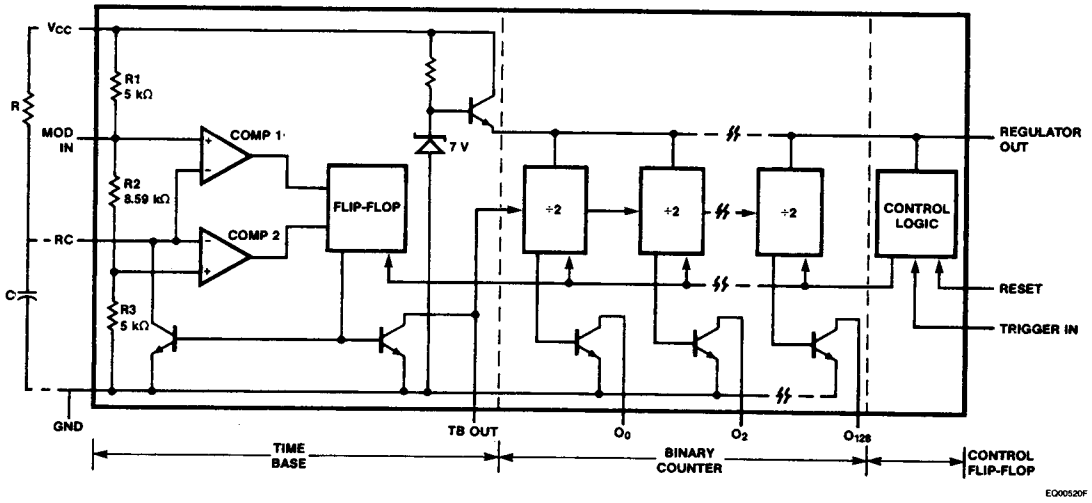
Block Diagram



μA2240C

Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, $R = 10$ kΩ, $C = 0.1$ μF, unless otherwise specified.

Symbol	Characteristic		Condition		Min	Typ	Max	Unit
General Characteristic								
V_{CC}	Supply Voltage		For $V_{CC} \leq 4.5$ V, Short Lead 15 to Lead 16		4.0		15	V
I_{CC}	Supply Current	Total Circuit	$V_{CC} = 5.0$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V			4.0	7.0	mA
			$V_{CC} = 15$ V, $V_{TR} = 0$ V, $V_{RS} = 5.0$ V			13	18	
		Counter Only				1.5		
V_{REG}	Regulator Output		Measured at Lead 15	$V_{CC} = 5.0$ V	3.9	4.4		V
				$V_{CC} = 15$ V	5.8	6.3	6.8	
Time-Base								
t_{ACC}	Timing Accuracy[1]		$V_{RS} = 0$, $V_{TR} = 5.0$ V			3.5	5.0	%
$\Delta t/\Delta T$	Temperature Drift		$0°C \leq T_J \leq 75°C$	$V_{CC} = 5.0$ V		200		ppm/°C
				$V_{CC} = 15$ V		80		
$\Delta t/\Delta V$	Supply Drift		$V_{CC} \geq 8.0$ V (See Performance Curves)			0.08	0.3	%/V
f_{Max}	Max Frequency		$R = 1.0$ kΩ, $C = 0.007$ μF			130		kHz
V_{MOD}	Modulation Voltage Level		Measured at Lead 12	$V_{CC} = 5.0$ V	2.80	3.50	4.20	V
				$V_{CC} = 15$ V		10.5		
R_T	Recommended Range of Timing Components Timing Resistor		(See Performance Curves)		0.001		10	MΩ

μA2240C (Cont.)
Electrical Characteristics $T_A = 25°C$, $V_{CC} = 5.0$ V, R = 10 kΩ, C = 0.1 μF, unless otherwise specified.

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
C_T	Timing Capacitor		0.01		1000	μF
Trigger/Reset Controls						
V_{TR}	Trigger Threshold	Measured at Lead 11, $V_{RS} = 0$ V		1.4	2.0	V
I_{TR}	Trigger Current	$V_{RS} = 0$ V, $V_{TR} = 2.0$ V		10		μA
Z_T	Trigger Impedance			25		kΩ
t_{RSPT}	Trigger Response Time[2]			1.0		μs
V_{RS}	Reset Threshold	Measured at Lead 10, $V_{TR} = 0$ V		1.4	2.0	V
I_R	Reset Current	$V_{TR} = 0$ V, $V_{RS} = 2.0$ V		10		μA
Z_R	Reset Impedance			25		kΩ
t_{RSPT}	Reset Response Time[2]			0.8		μs
Counter						
TR_{Max}	Max Toggle Rate	Measured at Lead 14 $V_{RS} = 0$ V, $V_{TR} = 5.0$ V		1.5		MHz
Z_I	Input Impedance			20		kΩ
V_{TH}	Input Threshold		1.0	1.4		V
t_r	Output Rise Time	Measured at Leads 1 through 8 $R_L = 3.0$ kΩ, $C_L = 10$ pF		180		ns
t_f	Fall Time			180		
I_{O-}	Sink Current	$V_{OL} \leq 0.4$ V	2.0	4.0		mA
I_{CEX}	Leakage Current	$V_{OH} = 15$ V		0.01	15	μA

Notes
1. Timing error solely introduced by μA2240 measured as % of ideal time-base period of T = RC.
2. Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Lead 1.

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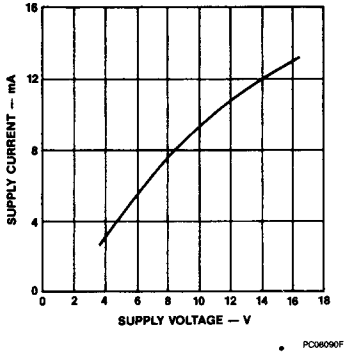
Typical Performance Curves

Supply Current vs Supply Voltage in Reset Condition



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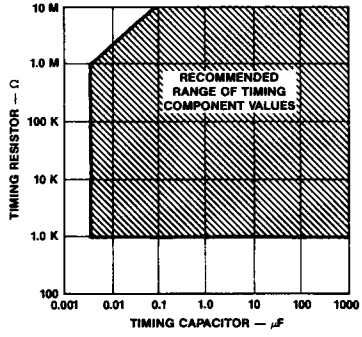
Recommended Range of Timing Component Values



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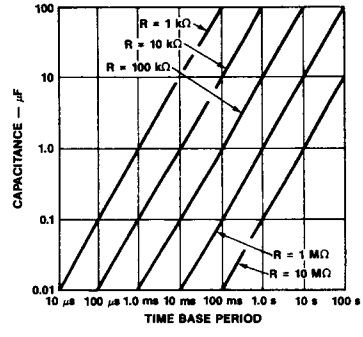
Time-Base Period vs External RC



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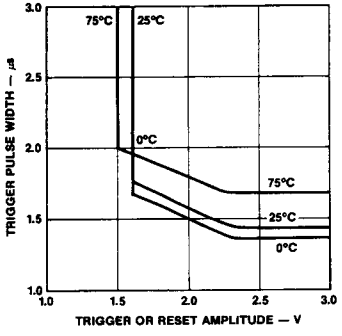
Minimum Trigger Pulse Width vs Trigger and Reset Amplitude



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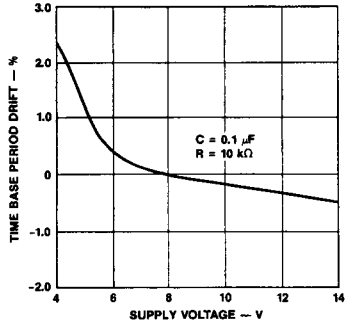
Time-Base Period Drift vs Supply Voltage



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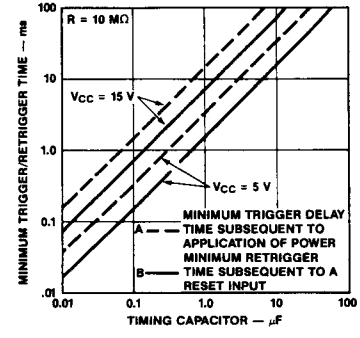
Minimum Trigger/Retrigger Timing vs Timing Capacitor



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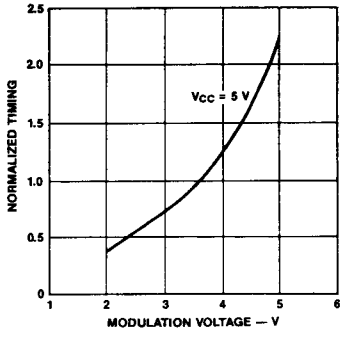
Normalized Change in Time-Base Period vs Modulation Voltage



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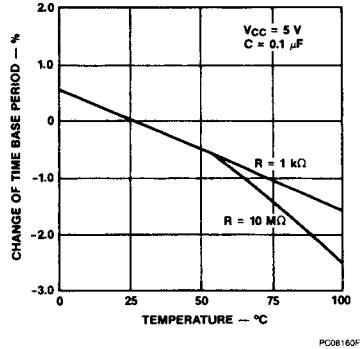
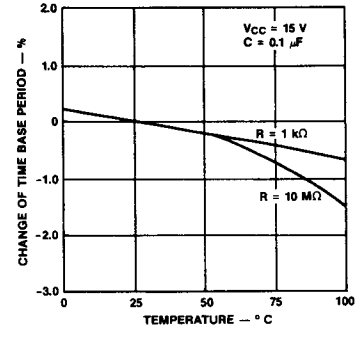
Time-Base Period vs Temperature



PC08160F

Time-Base Period vs Temperature



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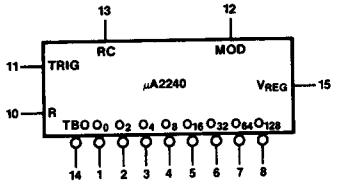
Functional Description

(*Figure 1* and Block Diagram)
When power is applied to the μA2240 with no trigger or reset inputs, the circuit starts with all outputs HIGH. Application of a positive going trigger pulse to trigger lead 11, initiates the timing cycle. The trigger input activates the time-base oscillator, enables the counter section and sets the counter outputs LOW. The time-base oscillator generates timing pulses with a period T = 1 RC. These clock pulses are counted by the binary counter section. The timing sequence is completed when a positive going reset pulse is applied to Reset, lead 10.

Once triggered, the circuit is immune from additional trigger inputs until the timing cycle is completed or a reset input is applied. If both the reset and trigger are activated simultaneously, the trigger takes precedence.

Figure 2 gives the timing sequence of output waveforms at various circuit terminals, subsequent to a trigger input. When the circuit is in a reset state, both the time-base and the counter sections are disabled and all the counter outputs are HIGH.

Figure 1 Logic Symbol



V_{CC} = Lead 16
GND = Lead 9

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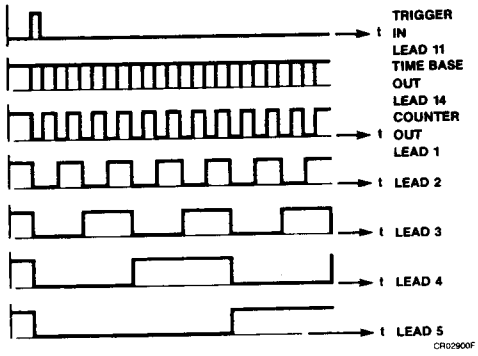
Figure 2 Timing Diagram of Output Waveforms



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In most timing applications, one or more of the counter outputs are connected to the reset terminal with S1 closed (*Figure 3*). The circuit starts timing when a trigger is applied and automatically resets itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S1 open), the circuit operates in an astable or free running mode, following a trigger input.

Important Operating Information

Ground connection is lead 9.

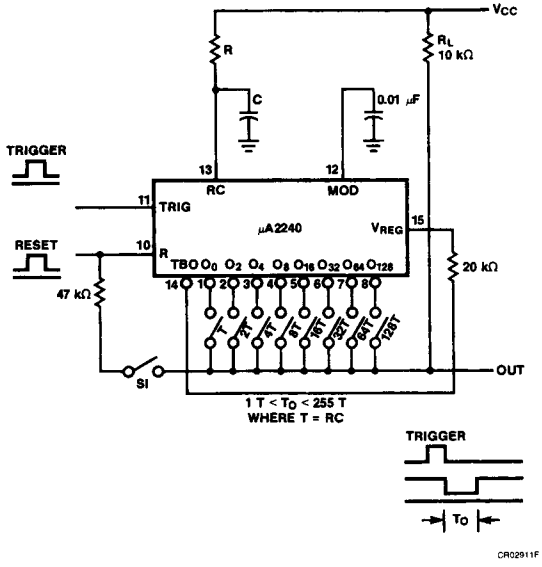
Reset (R) (lead 10) sets all outputs HIGH.

Trigger (TRIG) (lead 11) sets all outputs LOW.

Time-base output (TBO) (lead 14) can be disabled by bringing the RC input (lead 13) LOW via a 1.0 kΩ resistor.

Normal TBO (lead 14) is a negative going pulse greater than 500 ns.

Figure 3 Basic Circuit Connection for Timing Applications Monostable: S1 Closed Astable: S1 Open



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Note: Under the conditions of high supply voltages ($V_{CC} > 7.0$ V) and low values of timing capacitor ($C_T < 0.1\mu F$), the pulse width of TBO may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from TBO (lead 14) to ground (lead 9).

Reset (lead 10) stops the time-base oscillator.

Outputs ($O_0 \ldots O_{128}$) (leads 1 – 8) sink 2.0 mA current with $V_{OL} \leq 0.4$ V.

For use with external clock, minimum clock pulse amplitude should be 3.0 V, with greater than 1.0 μs pulse duration.

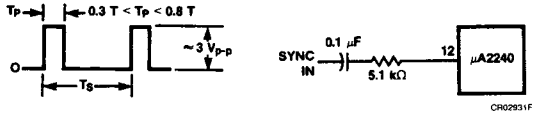
Circuit Controls

Counter Outputs ($O_0 \ldots O_{128}$, leads 1 thru 8)
The binary counter outputs are buffered open collector type stages, as shown in the block diagram. Each output is capable of sinking 2.0 mA at 0.4 V V_{OL}. In the reset condition, all the counter outputs are HIGH or in the non-conducting state. Following a trigger input, the outputs change state in accordance with the timing diagram of *Figure 2.* The counter outputs can be used individually, or can be connected together in a wired-OR configuration, as described in the programming segment of this data sheet.

Reset and Trigger Inputs (R and TRIG, 10 and 11)
The circuit is reset or triggered with positive going control pulses applied to leads 10 and 11 respectively. The threshold level for these controls is approximately two diode drops (≈ 1.4 V) above ground. Minimum pulse widths for reset and trigger inputs are shown in the Performance Curves. Once triggered, the circuit is immune to additional trigger inputs until the end of the timing cycle.

Modulation and Sync Input (MOD, lead 12)
The oscillator time-base period (T) can be modulated by applying a DC voltage to MOD, lead 12 (see Performance Curves). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to MOD, lead 12, as shown in *Figure 4.* Recommended sync pulse widths and amplitudes are also given.

Figure 4 Operation with External Sync Signal



The time-base can be synchronized by setting T to be an integer multiple of the sync pulse period (T_S). This can be done by choosing the timing components R and C at lead 13 such that:

$$T = RC = (T_S/m)$$

where:

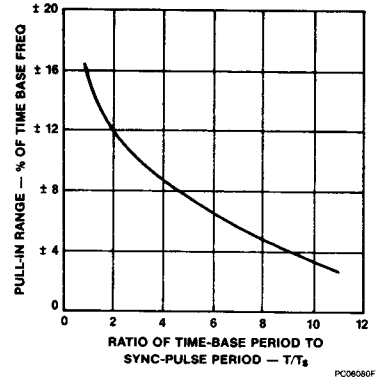
m is an integer, $1.0 \leq m \leq 10$

Figure 5 gives the typical pull-in range for harmonic synchronization for various values of harmonic modulus, m. For $m < 10$, typical pull-in range is greater than ±4% of time-base frequency.

RC Terminal (lead 13)
The time-base period T is determined by the external RC network connected to RC, lead 13. When the time-base is triggered, the waveform at lead 13 is an exponential ramp with a period T = 1 RC.

Time-Base Output (TBO, lead 14)
The time-base output is an open-collector type stage as shown in the block diagram, and requires a 20 kΩ pull-up resistor to lead 15 for proper circuit operation. In the reset state, the time-base output is HIGH. After triggering, it produces a negative going pulse train with a period T = RC, as shown in the diagram of *Figure 2.* The time-base output is internally connected to the binary counter section and can also serve as the input for the external clock signal when the circuit is operated with an external time base. The counter section triggers on the negative going edge of the timing or clock pulses generated at TBO, lead 14. The trigger threshold for the counter section is

Figure 5 Typical Pull-in Range for Harmonic Synchronization

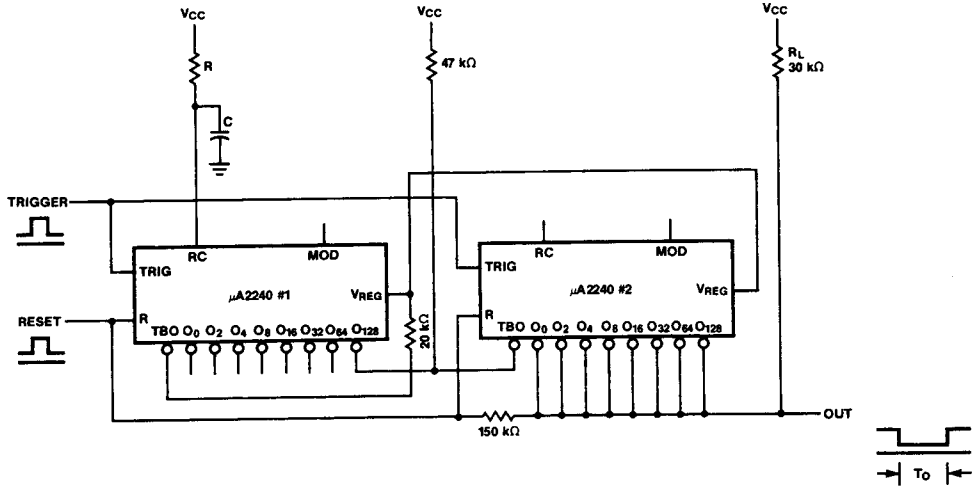


≈ +1.4 V. The counter section can be disabled by clamping the voltage level at lead 14 to ground.

When using high supply voltages (V_{CC} > 7.0 V) and a small value timing capacitor (C_T < 0.1 μF), the pulse width at TBO lead 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 600 pF capacitor from lead 14 to ground.

Regular Output (V_{REG}, lead 15)
The regulator output V_{REG} is used internally to drive the binary counter and the control logic. This terminal can also be used as a supply to additional μA2240 circuits when several timer circuits are cascaded *(see Figure 6)* to minimize power dissipation. For circuit operation with an external clock, V_{REG} can be used as the V_{CC} input terminal to power down the internal time-base and reduce power dissipation. When supply voltages less than 4.5 V are used with the internal time-base, lead 15 should be shorted to lead 16.

Figure 6 Low Power Operation of Cascaded Timers



VCC = Lead 16
GND = Lead 9

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Monostable Operation

Precision Timing
In precision timing applications, the μA2240 is used in its monostable or self-resetting mode. The generalized circuit connection for this application is shown in *Figure 3.* The output is normally HIGH and goes LOW following a trigger input. It remains LOW for the time duration (T_O) and then returns to the HIGH state. The duration of the timing cycle T_O is given as:

$$T_O = nT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at RC lead 13 (see Performance Curves) and n is an integer in the range of $1 \leqslant n \leqslant 255$ as determined by the combination of counter outputs ($O_0 \ldots O_{128}$), leads 1 through 8, connected to the output bus.

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Counter Output Programming

The binary counter outputs, $O_0 \ldots O_{128}$, leads 1 through 8 are open collector type stages and can be shorted together to a common pull-up resistor to form a wired-OR connection; the combined output will be LOW as long as any one of the outputs is LOW. The time delays associated with each counter output can be added together. This is done by simply shorting the outputs together to form a common output bus as shown in *Figure 3*. For example, if only lead 6 is connected to the output and the rest left open, the total duration of the timing cycle, T_O, is 32 T. Similarly, if leads 1, 5, and 6 are shorted to the output bus, the total time delay is $T_O = (1 + 16 + 32)\ T = 49\ T$. In this manner, by proper choice of counter terminals connected to the output bus, the timing cycle can be programmed to be $1\ T \leqslant T_O \leqslant 255\ T$.

Ultra Long Time Delay Application

Two μA2240 units can be cascaded as shown in *Figure 7* to generate extremely long time delays. Total timing cycle of two cascaded units can be programmed from $T_O = 256$ RC to $T_O = 65{,}536$ RC in 256 discrete steps by selectively shorting one or more of the counter outputs from Unit 2 to the output bus. In this application, the reset and the trigger terminals of both units are tied together and the Unit 2 time base is disabled. Normally, the output is HIGH when the system is reset. On triggering, the output goes LOW where it remains for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator.

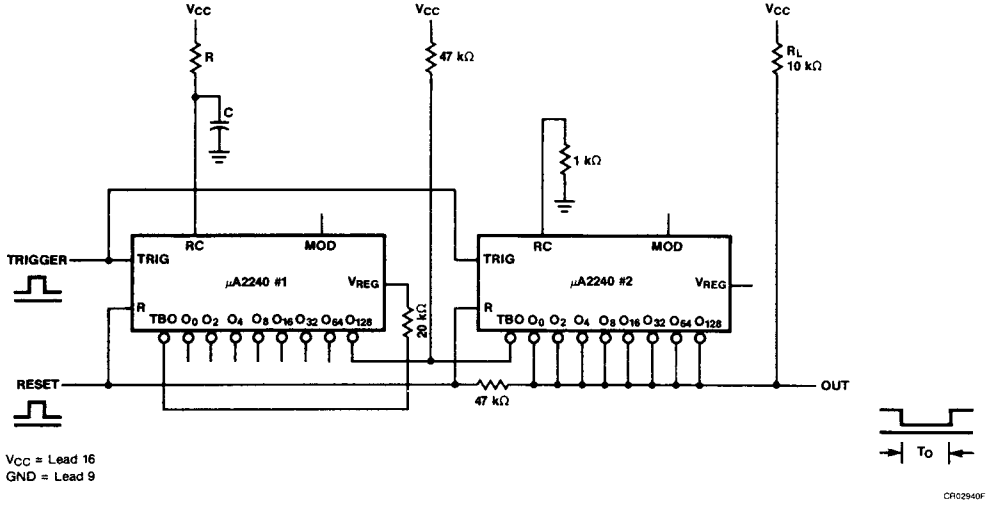
In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption by using the circuit connection of *Figure 6*. In this case, the V_{CC} terminal (lead 16) of Unit 2 is left open, and the second unit is powered from the regulator output of Unit 1 by connecting the V_{REG} (lead 15) of both units together.

Astable Operation

The μA2240 can be operated in its astable or free running mode by disconnecting the reset terminal (lead 10) from the counter outputs. Two typical circuits are shown in *Figures 8* and *9*. The circuit in *Figure 8* operates in its free running mode with external trigger and reset signals. It starts counting and timing following a trigger input until an external reset pulse is applied. Upon application of a positive going reset signal to lead 10, the circuit reverts back to its reset state. This circuit is essentially the same as that of *Figure 3* with the feedback switch S1 open.

The circuit of *Figure 9* is designed for continuous operation. It self triggers automatically when the power supply is turned on, and continues to operate in its free running mode indefinitely. In astable or free running operation, each of the counter outputs can be used individually as synchronized oscillators, or they can be interconnected to generate complex pulse patterns.

Figure 7 Cascaded Operation for Long Delays



Binary Pattern Generation

In astable operation, as shown in *Figure 8*, the output of the μA2240 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of *Figure 2* which shows the phase relations between the counter outputs. *Figures 10* and *11* show some of the complex pulse patterns that can be generated. The pulse pattern repeats itself at a rate equal to the period of the highest counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the lowest counter bit connected to the output.

Figure 8 Operation with Trigger and Reset Inputs (Note 1)

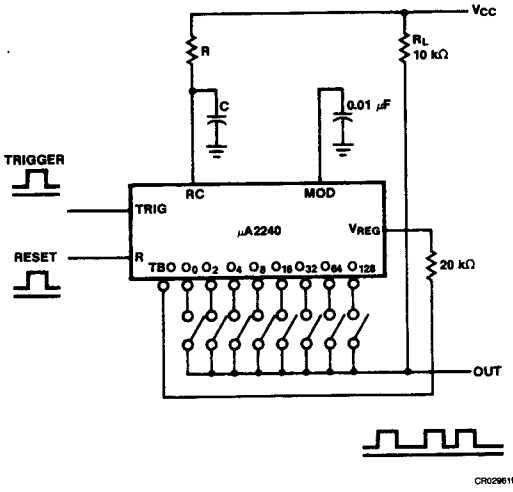


Figure 9 Free Running or Continuous Operation (Note 1)

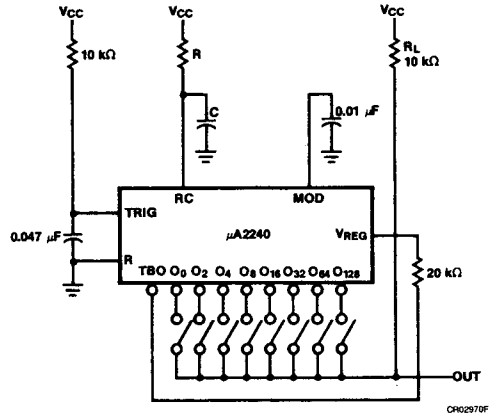
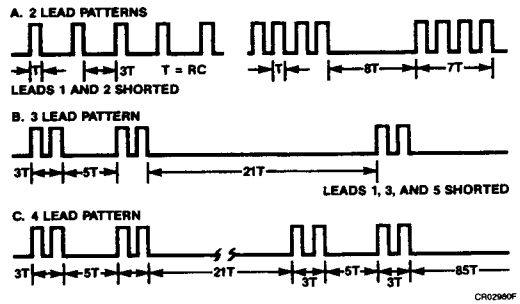


Figure 10 Binary Pulse Patterns Obtained by Shorting Various Counter Outputs



Note

1. V_{CC} = Lead 16
   GND = Lead 9

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Figure 11 Continuous Free run Operation Examples of Output