

**5.1V AND ADJUSTABLE VOLTAGE REGULATOR
WITH DISABLE AND RESET**

- OUTPUT CURRENTS UP TO 750mA
- FIXED PRECISION OUTPUT 1 VOLTAGE 5.1V ± 2%
- OUTPUT 2 VOLTAGE PROGRAMMABLE FROM 2.8 TO 16V
- OUTPUT 1 WITH RESET FACILITY
- OUTPUT 2 WITH DISABLE BY TTL INPUT
- SHORT CIRCUIT PROTECTION AT BOTH OUTPUTS
- THERMAL PROTECTION
- LOW DROP OUTPUT VOLTAGE

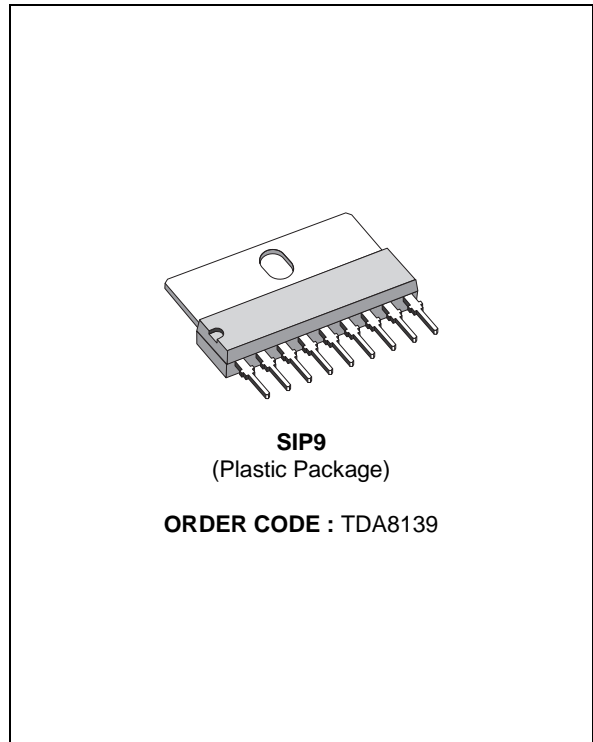
DESCRIPTION

The TDA8139 is a monolithic dual positive voltage regulator designed to provide precision output voltages of 5.1V and adjustable at currents up to 750mA.

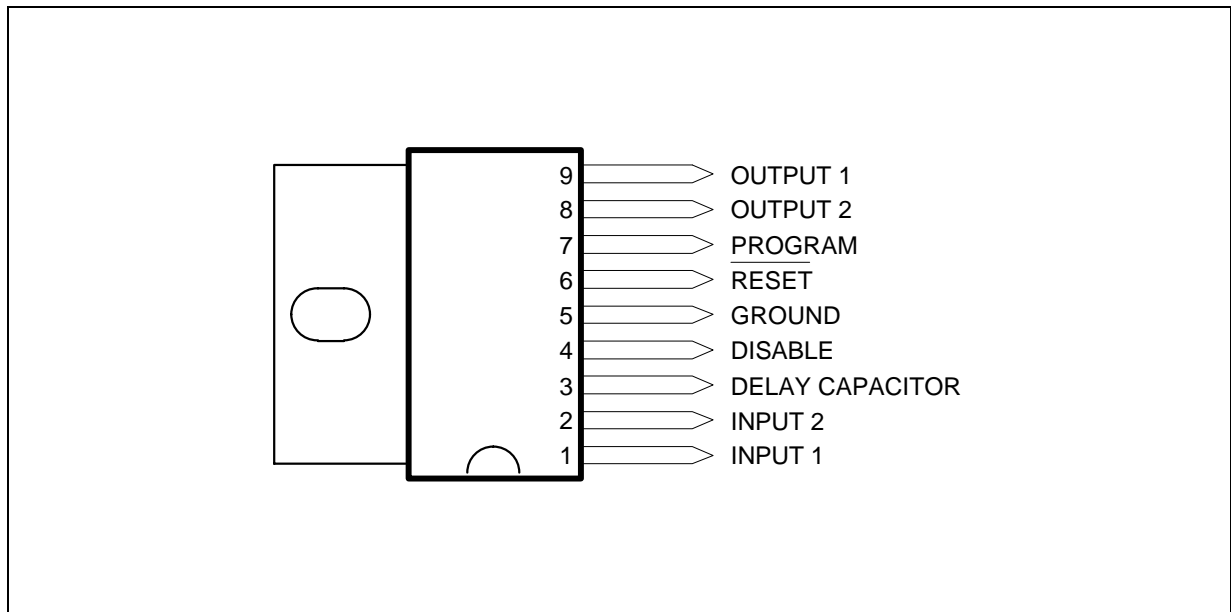
An internal reset circuit generates a reset pulse when the output 1 decrease below the regulated voltage value.

Output 2 can be disabled by TTL input.

Short circuit and thermal protections are included.

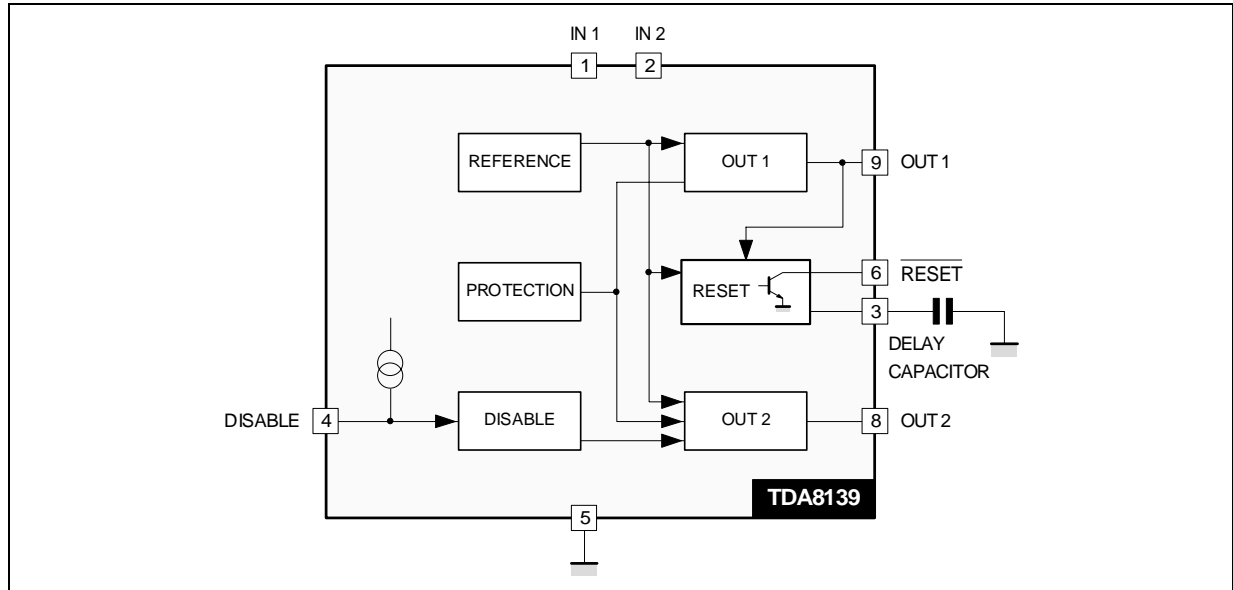


PIN CONNECTIONS



8139-01:EPS

BLOCK DIAGRAM



8139-02.EPS

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1, 2	20	V
V_{DIS}	Disable Input Voltage Pin 4	20	V
V_{RST}	Output Voltage at Pin 6	20	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	- 65 to + 150	°C
T_J	Junction Temperature	0 to + 150	°C

8139-01.TBL

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(j-c)}$	Thermal Resistance Junction-case	Max. 8	°C/W
T_J	Recommended Junction Temperature	Max. 130	°C

8139-02.TBL

ELECTRICAL CHARACTERISTICS ($V_{IN} = 7V$; $T_j = 25^{\circ}C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	$I_{O1} = 10mA$	5	5.1	5.2	V
V_{O2}	Output Voltage	$I_{O2} = 10mA$	2.8		16	V
$V_{IO1, 2}$	Dropout Voltage	$I_{O1, 2} = 750mA$			1.4	V
V_{O1}	Line Regulation 1	$7V < V_{IN1} < 14V, 12V < V_{IN2} < 18V, @ V_{O2} : 10V, I_{O1, 2} = 200mA$			50	mV
V_{O2}	Line Regulation 2				100	mV
V_{O1}	Load Regulation 1	$5mA < I_{O1, 2} < 0.6A, @ V_{O2} = 10V$			100	mV
V_{O2}	Load Regulation 2				200	mV
I_Q	Quiescent Current	$I_{O1} = 10mA, \text{Output 2 Disabled}$			2	mA
V_{O1RST}	Reset Threshold Voltage	$(K = V_{O1})$	$K - 0.4$	$K - .25$	$K - 0.1$	V
V_{RTH}	Reset Threshold Hysteresis	(see circuit description)	20	50	75	mV
t_{RD}	Reset Pulse Delay at Pin 6	$C_e = 100nF$ (see circuit description)		25		ms

8139-03.TBL

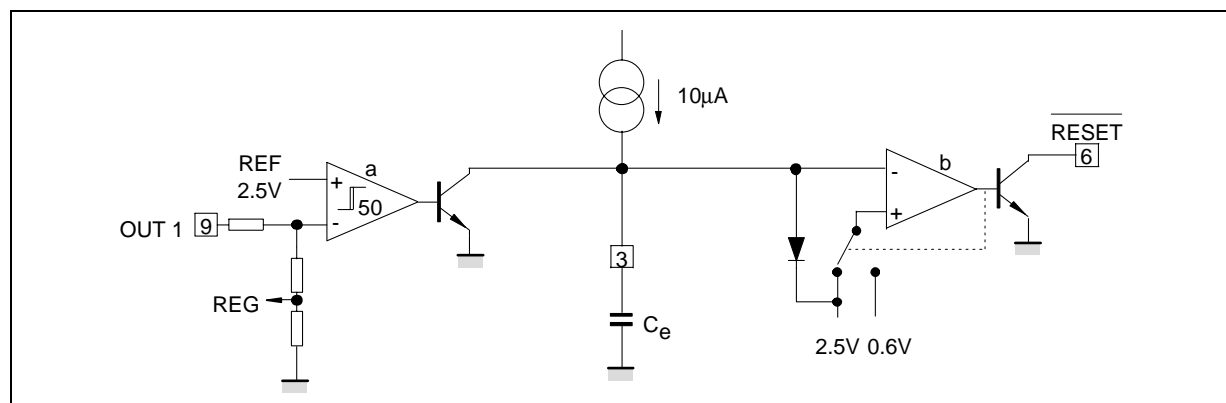
ELECTRICAL CHARACTERISTICS ($V_{IN} = 7V$; $T_j = 25^\circ C$ unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition	$I_5 = 5mA$			0.4	V
I_{RH}	Leakage Current at Pin 6 in Normal Condition	$V_5 = 10V$			10	μA
$K_{O1,2}$	Output Volt. Thermal Drift	$K_0 = \frac{\Delta V_o \cdot 10^6}{\Delta T \cdot V_o}$ $T_j = 0 \text{ to } +125^\circ C$		100		ppm/ $^\circ C$
$I_{O1,2 \text{ sc}}$	Short Circ. Ouput Current	$V_{IN} = 7V$			1.6	A
		$V_{IN} = 16V$, (see note 1)			1	A
V_{DISH}	Disable Volt. at Pin 4 High (out 2 active)		2			V
V_{DISL}	Disable Volt. at Pin 4 Low (out 2 disabled)				0.8	V
I_{DIS}	Disable Bias Current at Pin 4	$0V < V_{DIS} < 7V$	-100		2	μA
V_{ref}	Pin 7			2.5		V
$T_{j\text{sd}}$	Junction Temp. for Thermal Shut Down			145		$^\circ C$

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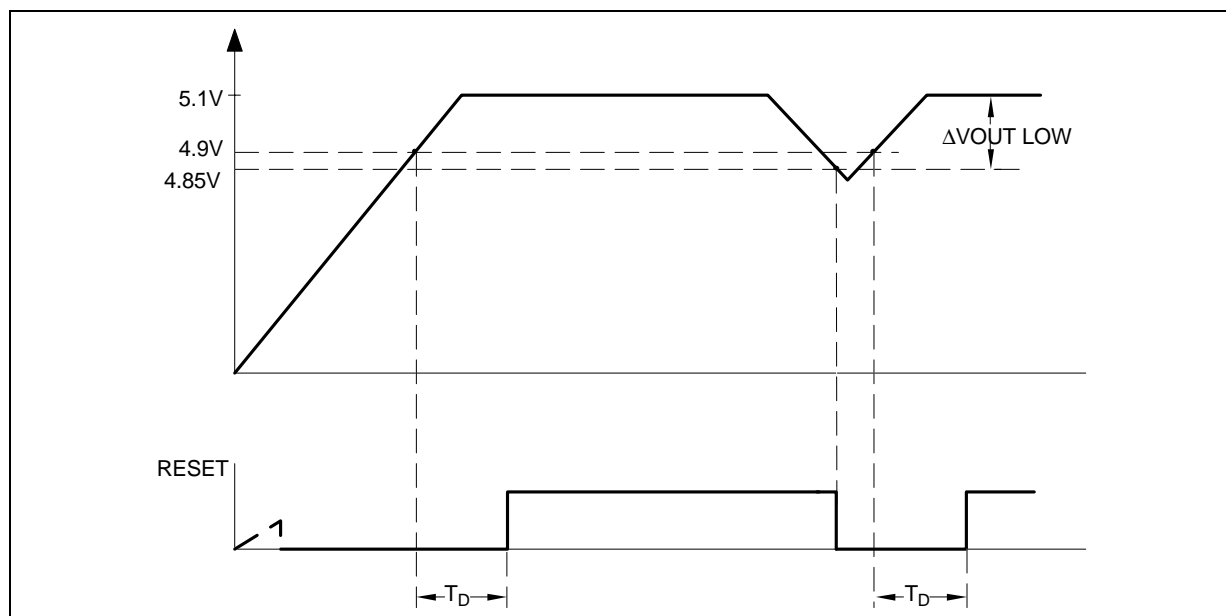
Note 1 : The output short circuit currents are tested one channel at time. During a short circuit a large consumption of power occurs, but the thermal protection circuit prevents any excessive temperature. Safe permanent short-circuit is only guaranteed for input voltages up to 16V.

Figure 1



8139-03.EPS

Figure 2



8139-04.EPS

CIRCUIT DESCRIPTION

The TDA8139 is a dual voltage regulator with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS test. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}), the regulator 2 will not work if the Pin 1 is not supplied.

The outputs stages have been realized in darlington configuration with a drop typical of 1.2V.

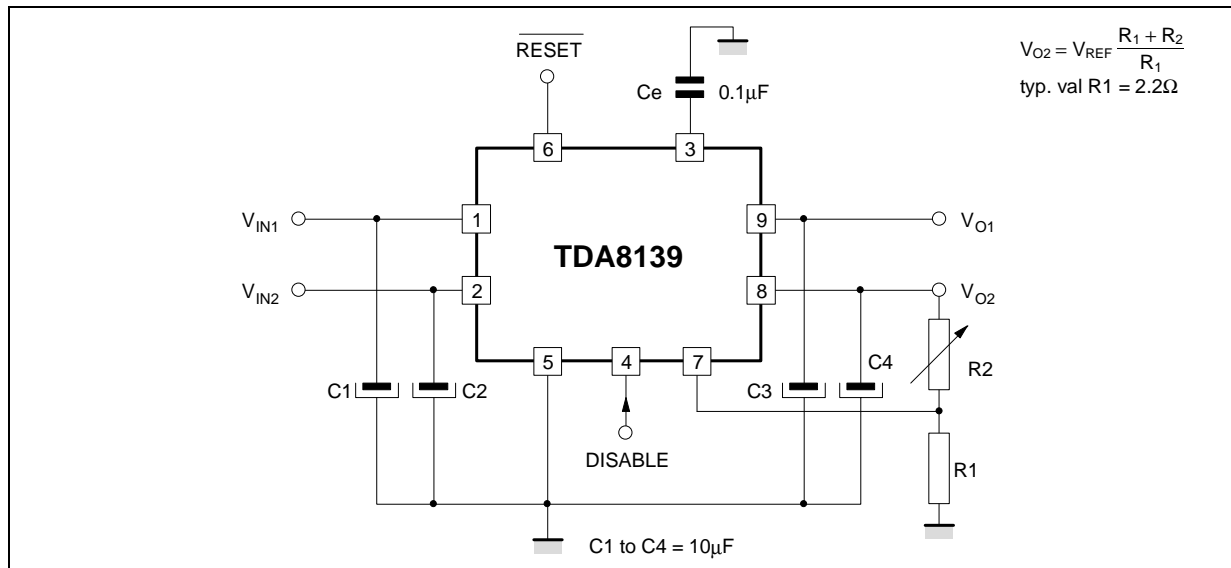
The disable circuit, switch-off the output 2 if a voltage lower than 0.8V is applied at pin 4.

The Reset circuit checks the voltage at the output 1. If this one goes below $V_{OUT} - 0.25V$ (4.85V Typ.), the comparator "a" (see Figure 1) discharges rapidly the capacitor C_e and the reset output goes at once low. When the voltage at the OUT 1 rises above $V_{OUT} - 0.2V$ (4.9V Typ.), the voltage V_{C_e} increases linearly to 2.5V corresponding to a delay

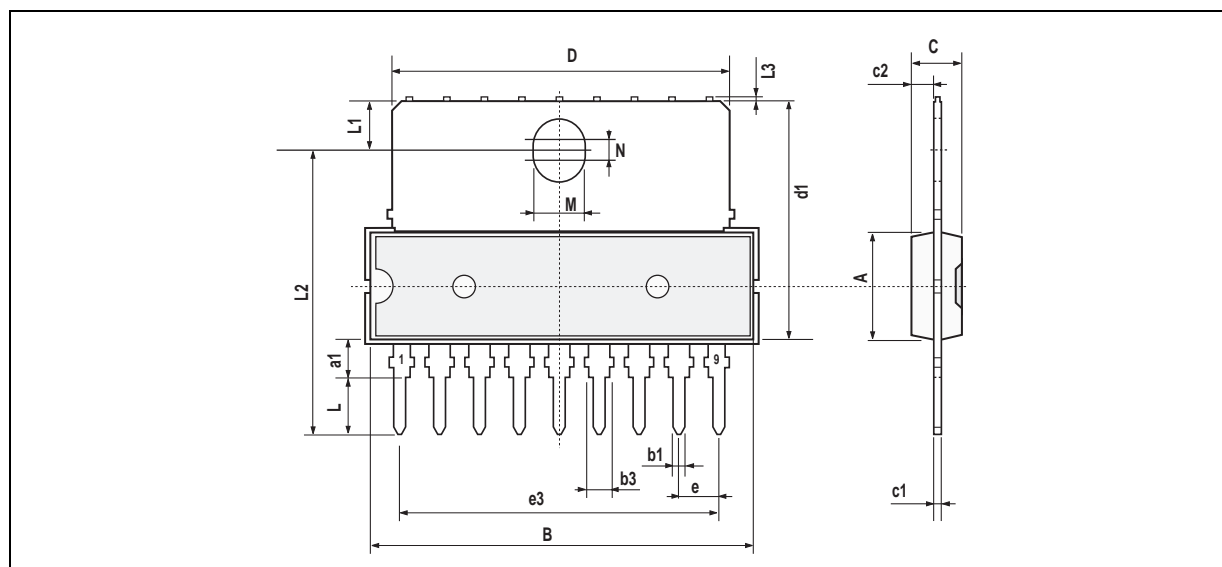
$$t_d \text{ following the low : } t_d = \frac{C_e \cdot 2.5V}{10\mu A} \text{ (see figure 2),}$$

then the reset output goes high again. To avoid glitches in the reset output, the second comparator "b" has a large hysteresis (1.9V).

TYPICAL APPLICATION



8139-05.EPS

PACKAGE MECHANICAL DATA
 9 PINS - PLASTIC SIP


PM-SIP9.EPS

Dimensions	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			0.122		
L1		3			0.118	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	

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