INTEGRATED CIRCUITS

DATA SHEET

TDA6107Q
Triple video output amplifier

Preliminary specification
Supersedes data of 1997 Aug 25
File under Integrated Circuits, IC02

1998 Jun 08

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FEATURES

- Typical bandwidth of 5.0 MHz for an output signal of 60 V (peak-to-peak value)
- High slew rate of 900 V/μs
- No external components required
- Very simple application
- Single supply voltage of 200 V
- Internal reference voltage of 2.5 V
- Fixed gain of 52
- Black-Current Stabilization (BCS) circuit
- Thermal protection.

GENERAL DESCRIPTION

The TDA6107Q includes three video output amplifiers in one plastic DIL-bent-SIL 9-pin medium power (DBS9MPF) package (SOT111-1), using high-voltage DMOS technology, and is intended to drive the three cathodes of a colour CRT directly. To obtain maximum performance, the amplifier should be used with black-current control.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6107Q	DBS9MPF	plastic DIL-bent-SIL medium power package with fin; 9 leads	SOT111-1

BLOCK DIAGRAM

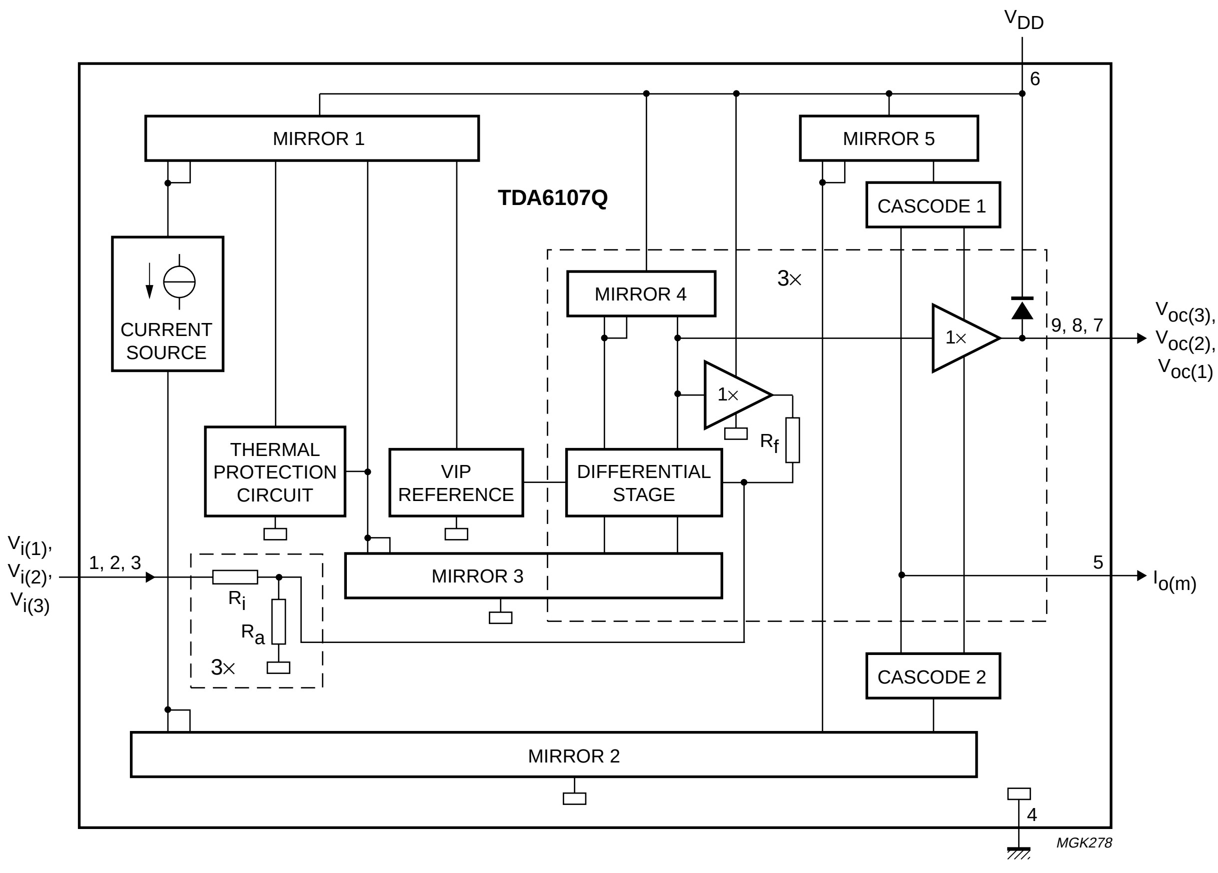


Fig.1 Block diagram (one amplifier shown).

PINNING

SYMBOL	PIN	DESCRIPTION
$V_{i(1)}$	1	inverting input 1
$V_{i(2)}$	2	inverting input 2
$V_{i(3)}$	3	inverting input 3
GND	4	ground (fin)
I_{om}	5	black current measurement output
V_{DD}	6	supply voltage
$V_{oc(3)}$	7	cathode output 3
$V_{oc(2)}$	8	cathode output 2
$V_{oc(1)}$	9	cathode output 1

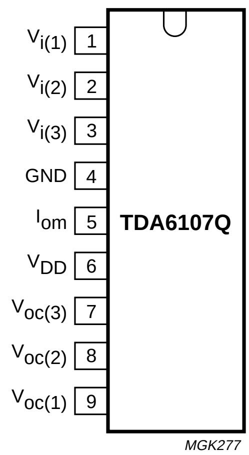


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages measured with respect to pin 4 (ground); currents as specified in Fig.1; unless otherwise specified.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	0	250	V
V_i	input voltage at pins 1 to 3	0	12	V
$V_{o(m)}$	measurement output voltage	0	6	V
$V_{o(c)}$	cathode output voltage	0	V_{DD}	V
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	–20	+150	°C
V_{es}	electrostatic handling			
	Human Body Model (HBM)	–	1000	V
	Machine Model (MM)	–	300	V

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see *"Handling MOS Devices"*).

QUALITY SPECIFICATION

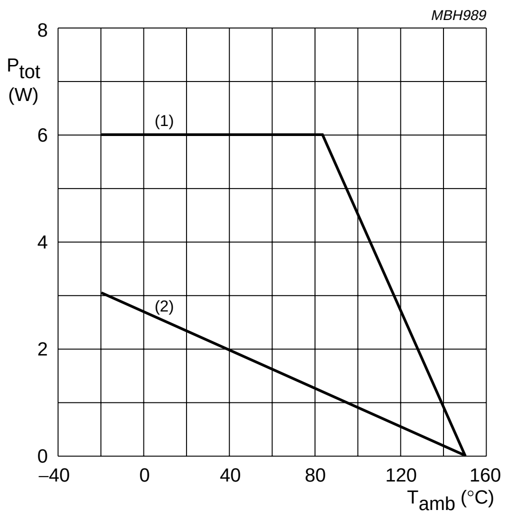
Quality specification *"SNW-FQ-611 part E"* is applicable and can be found in the *"Quality reference Handbook"*. The handbook can be ordered using the code 9397 750 00192.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient		56	K/W
$R_{th\ j\text{-}fin}$	thermal resistance from junction to fin	note 1	11	K/W
$R_{th\ h\text{-}a}$	thermal resistance from heatsink to ambient		18	K/W

Note

1. An external heatsink is necessary.



(1) Infinite heatsink.
(2) No heatsink.

Fig.3 Power derating curves.

Thermal protection

The internal thermal protection circuit gives a decrease of the slew rate at high temperatures: 10% decrease at 130 °C and 30% decrease at 145 °C (typical values on the spot of the thermal protection circuit).

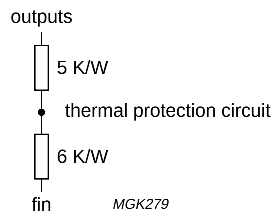


Fig.4 Equivalent thermal resistance network.

CHARACTERISTICS

Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V. Test conditions: T_{amb} = 25 °C; V_{DD} = 200 V; $V_{o(c1)} = V_{o(c2)} = V_{o(c3)} = \frac{1}{2}V_{DD}$; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th\ h\text{-}a}$ = 18 K/W (measured in test circuit of Fig.9); unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_q	quiescent supply current		6.2	7.2	8.2	mA
$V_{ref(int)}$	internal reference voltage (input stage)		–	2.5	–	V
R_i	input resistance		–	3.6	–	kΩ
G	gain of amplifier		–	52	–	
ΔG	gain difference		–2.5	0	+2.5	
$V_{O(c)}$	nominal output voltage at pins 7, 8 and 9 (DC value)	I_i = 0 µA	120	130	140	V
$\Delta V_{O(c)(offset)}$	differential nominal output offset voltage between pins 7 and 8, 8 and 9 and 9 and 7 (DC value)	I_i = 0 µA	–	0	5	V
$\Delta V_{o(c)(T)}$	output voltage temperature drift at pins 7, 8 and 9		–	–10	–	mV/K
$\Delta V_{o(c)(T)(offset)}$	differential output offset voltage temperature drift between pins 7 and 8, 8 and 9 and 7 and 9		–	0	–	mV/K
$I_{o(m)(offset)}$	offset current of measurement output	$I_{o(c)}$ = 0 µA; 1.5 V < V_i < 5.5 V; 3 V < $V_{o(m)}$ < 6 V	–50	–	+50	µA
$\Delta I_{o(m)}/\Delta I_{o(c)}$	linearity of current transfer	–100 µA < $I_{o(c)}$ < 100 µA; 1.5 V < V_i < 5.5 V; 3 V < $V_{o(m)}$ < 6 V	0.9	1.0	1.1	
$I_{o(c)(max)}$	maximum peak output current (pins 7, 8 and 9)	50 V < $V_{o(c)}$ < V_{DD} – 50 V	–	20	–	mA
$V_{o(c)(min)}$	minimum output voltage (pins 7, 8 and 9)	V_i = 7.0 V; note 1	–	–	10	V
$V_{o(c)(max)}$	maximum output voltage (pins 7, 8 and 9)	V_i = 1.0 V; note 1	V_{DD} – 15	–	–	V
B_S	small signal bandwidth (pins 7, 8 and 9)	$V_{o(c)(p-p)}$ = 60 V (peak-to-peak value)	–	5	–	MHz
B_L	large signal bandwidth (pins 7, 8 and 9)	$V_{o(c)(p-p)}$ = 100 V (peak-to-peak value)	–	4.5	–	MHz
t_{Pco}	cathode output propagation time 50% input to 50% output (pins 7, 8 and 9)	$V_{o(c)(p-p)}$ = 100 V (peak-to-peak value) square wave; f <1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	60	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Δt_{Pco}	difference in cathode output propagation time 50% input to 50% output (pins 7 and 8, 7 and 9 and 8 and 9)	$V_{o(c)(p-p)}$ = 100 V (peak-to-peak value) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–10	0	+10	ns
$t_{o(r)}$	cathode output rise time 20% output to 80% output (pins 7, 8 and 9)	$V_{o(c)}$ = 50 to 150 V square wave; f < 1 MHz; t_f = 40 ns (pins 1, 2 and 3); see Fig.6 and note 2	50	68	85	ns
$t_{o(f)}$	cathode output fall time 80% output to 20% output (pins 7, 8 and 9)	$V_{o(c)}$ = 150 to 50 V square wave; f < 1 MHz; t_r = 40 ns (pins 1, 2 and 3); see Fig.7 and note 2	50	68	85	ns
t_{st}	settling time 50% input to 99% < output < 101% (pins 7, 8 and 9)	$V_{o(c)(p-p)}$ = 100 V (peak-to-peak value) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7	–	–	350	ns
SR	slew rate between 50 V to (V_{DD} – 50 V) (pins 7, 8 and 9)	$V_{i(p-p)}$ = 4 V (peak-to-peak value) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3)	–	900	–	V/µs
O_v	cathode output voltage overshoot (pins 7, 8 and 9)	$V_{o(c)(p-p)}$ = 100 V (peak-to-peak value) square wave; f < 1 MHz; $t_r = t_f$ = 40 ns (pins 1, 2 and 3); see Figs 6 and 7 and note 2	–	tbf	–	%
PSRR	power supply rejection ratio	f < 50 kHz; note 3	–	55	–	dB
$\alpha_{ct(DC)}$	DC crosstalk between channels		–	50	–	dB

Notes

1. See also Fig.5 for the typical DC-to-DC transfer of V_I to $V_{O(c)}$.
2. 20% and 80% have been used because of undershoot/slow settling.
3. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.

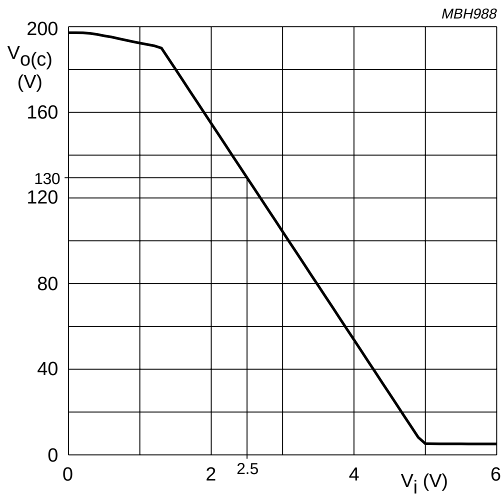


Fig.5 Typical DC-to-DC transfer of V_I to $V_{O(c)}$.

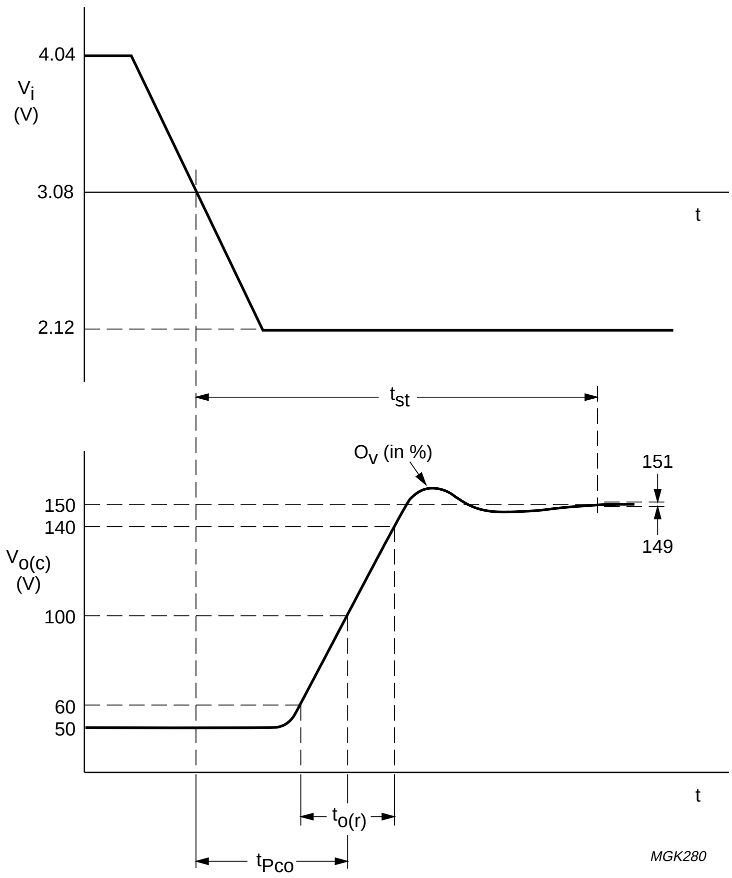


Fig.6 Output voltage (pins 7, 8 and 9) rising edge as a function of the AC input signal.

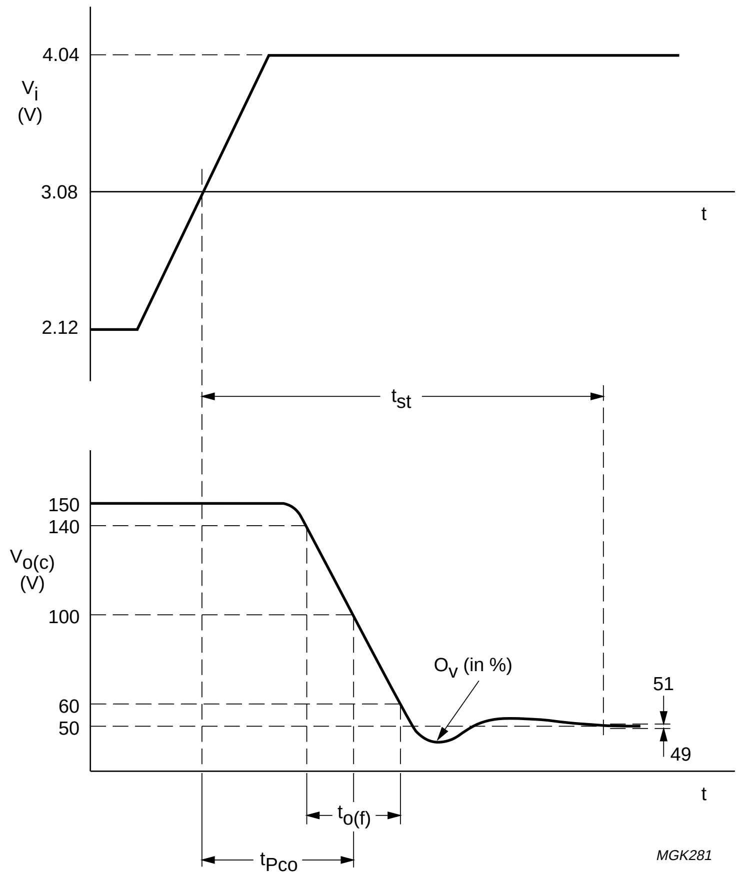


Fig.7 Output voltage (pins 7, 8 and 9) falling edge as a function of the AC input signal.

External flashover protection

For sufficient flashover protection it is necessary to apply an external diode and 100 Ω resistor for each channel. See for description the application note *"Application and Product description of TDA6107Q/N1"* (report number AN96072).

To limit the diode current an external 1 kΩ carbon high-voltage resistor in series with the external diode and a 2 kV spark gap are needed (for this resistor value, the CRT has to be connected to the main PCB).

V_{DD} must be decoupled to GND:

1. With a capacitor >20 nF with good HF behaviour (e.g. foil); this capacitance must be placed as close as possible to pins 6 and 4, but definitely within 5 mm
2. With a capacitor >3.3 μF on the picture tube base print.

Switch-off behaviour

The switch-off behaviour of the TDA6107Q is controllable. This is due to the fact that the output pins of the TDA6107Q are still under control of the input pins for low power supply voltages (approximately 30 V and higher).

Bandwidth

The addition of the flash resistor produces a decreased bandwidth and increases rise and fall times.

Dissipation

Regarding dissipation, distinction must first be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency).

The static dissipation of the TDA6107Q is due to voltage supply currents and load currents in the feedback network and CRT.

The static dissipation P_{stat} equals:

$$P_{stat} = V_{DD} \times I_{DD} + 3 \times V_{O(c)} \times I_{O(c)}$$

Where:

V_{DD} = supply voltage

I_{DD} = supply current

$V_{O(c)}$ = DC value of cathode voltage

$I_{O(c)}$ = DC value of cathode current.

The dynamic dissipation P_{dyn} equals:

$$P_{dyn} = 3 \times V_{DD} \times (C_L + C_{int}) \times f_i \times V_{o(c)(p\text{-}p)} \times \delta$$

Where:

C_L = load capacitance

C_{int} = internal load capacitance (≈4 pF)

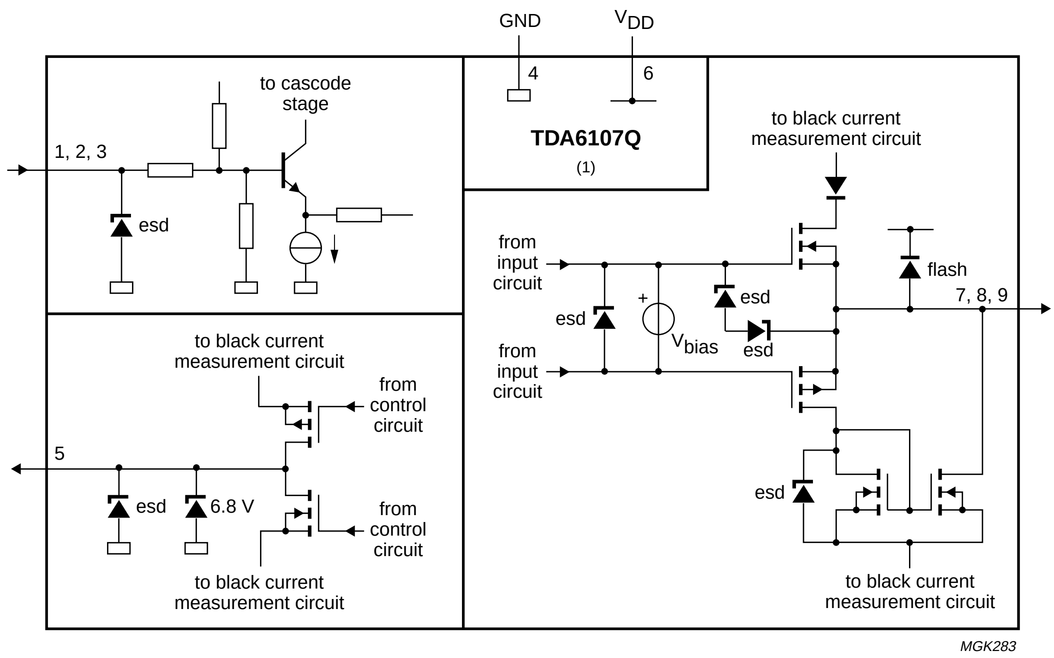
f_i = input frequency

$V_{o(c)(p\text{-}p)}$ = output voltage (peak-to-peak value)

δ = non-blanking duty cycle.

The IC must be mounted on the picture tube base print to minimize the load capacitance C_L.

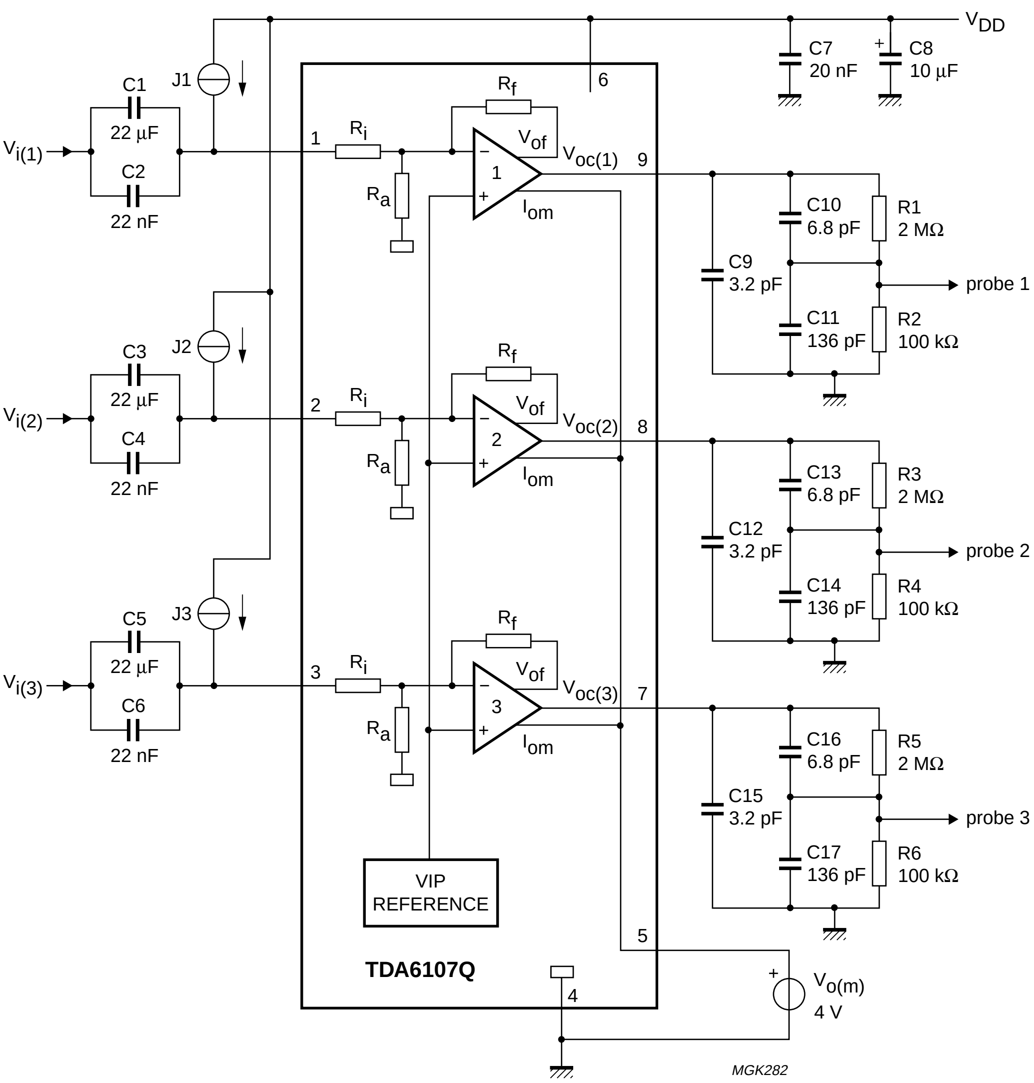
INTERNAL CIRCUITRY



(1) All pins have an energy protection for positive or negative overstress situations.

Fig.8 Internal pin configuration.

TEST AND APPLICATION INFORMATION

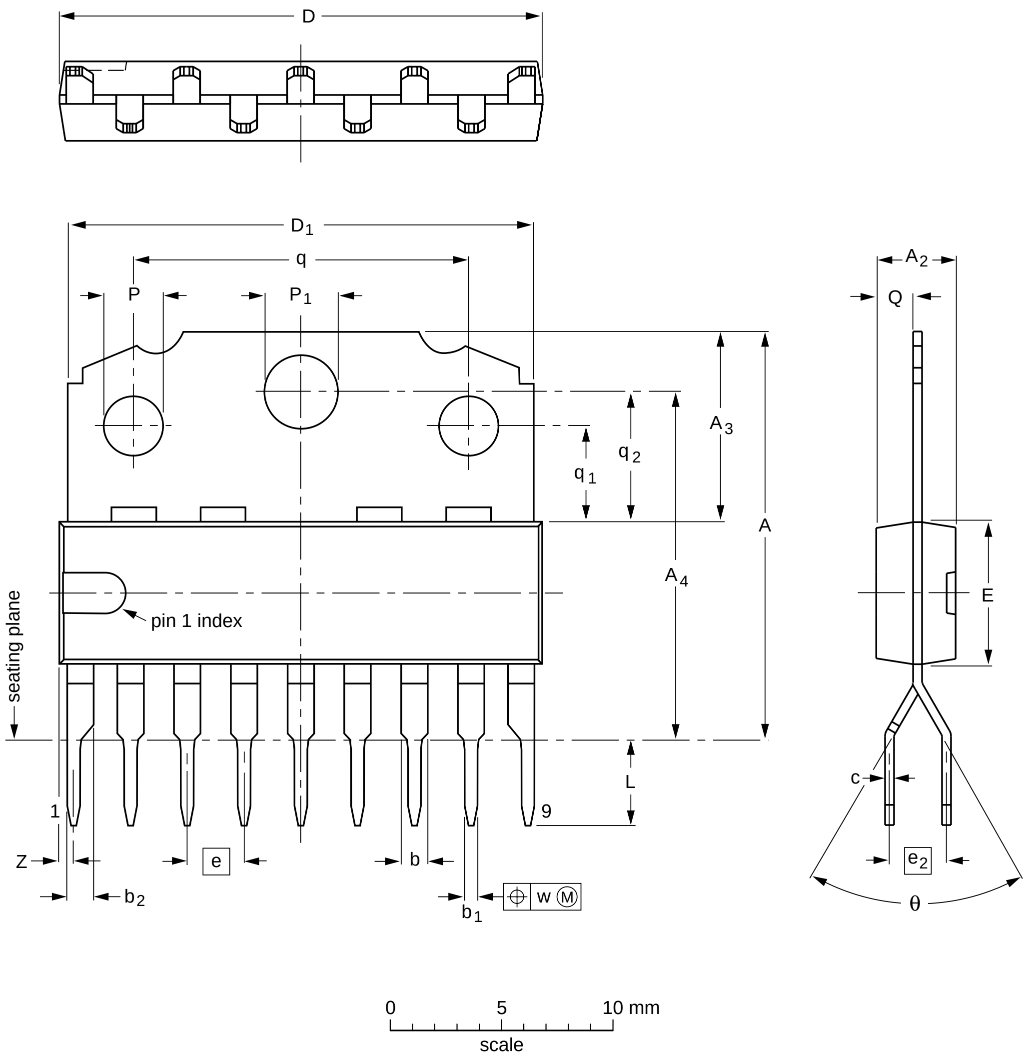


Current sources J1, J2 and J3 are to be tuned so that $V_{o(c)}$ of pins 9, 8 and 7 is set to 100 V.

Fig.9 Test circuit.

PACKAGE OUTLINE

DBS9MPF: plastic DIL-bent-SIL medium power package with fin; 9 leads **SOT111-1**

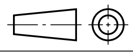


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2 max.	A_3	A_4	b	b_1	b_2	c	$D^{(1)}$	D_1	$E^{(1)}$	e	e_2	L	P	P_1	Q	q	q_1	q_2	w	$Z^{(1)}$ max.	θ
mm	18.5 17.8	3.7	8.7 8.0	15.5 15.1	1.40 1.14	0.67 0.50	1.40 1.14	0.48 0.38	21.8 21.4	21.4 20.7	6.48 6.20	2.54	2.54	3.9 3.4	2.75 2.50	3.4 3.2	1.75 1.55	15.1 14.9	4.4 4.2	5.9 5.7	0.25	1.0	65^o 55^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT111-1						~~92-11-17~~ 95-03-11

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Soldering by dipping or by wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Repairing soldered joints

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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