# TBA540

## REFERENCE COMBINATION

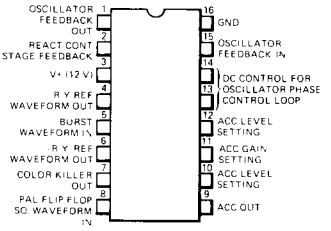
FAIRCHILD LINEAR INTEGRATED CIRCUIT



**GENERAL DESCRIPTION** — The TBA540 is an integrated reference oscillator circuit for PAL color television receivers. It incorporates an automatic phase and amplitude controlled crystal oscillator. The half-line frequency synchronous demodulator circuit compares the phases and amplitude of the swinging burst ripple with the PAL flip-flop waveform, and generates appropriate ACC, color killer and identification signals. The use of synchronous demodulation for these functions permits high noise immunity. This circuit is constructed on a single silicon chip using the Fairchild Planar* process.

- **COMPLETE SUBCARRIER REGENERATOR**
- **ACC AMPLIFIER**
- **COLOR KILLER**
- **AUTOMATIC PHASE CONTROL LOOP**

**CONNECTION DIAGRAM**
**16-PIN DIP**
(TOP VIEW)
PACKAGE OUTLINE 9B




**ORDER INFORMATION**

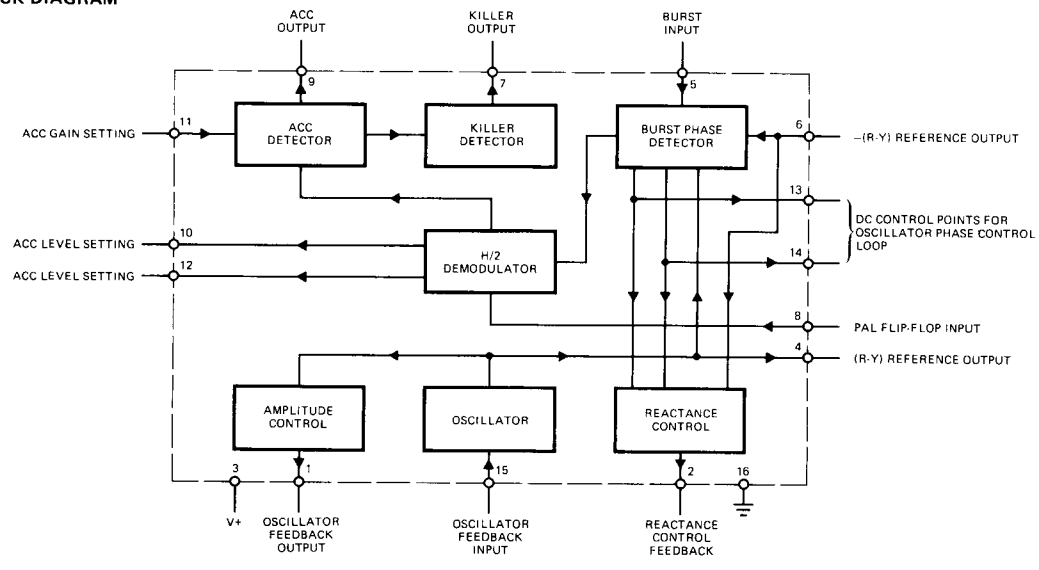
| TYPE | PART NO. |
|---|---|
| 540 | TBA540 |
| (540Q) | (TBA540Q)† |

†Not recommended for new designs.

**ABSOLUTE MAXIMUM RATINGS**

| | |
|---|---|
| Supply Voltage | 13.2 V |
| Total Power Dissipation at $T_A = 50^\circ C$ | 680 mW |
| Storage Temperature | −55 to +125° C |
| Operating Ambient Temperature | −20 to +60° C |
| Pin Temperature (Soldering, 10 s) | 260° C |

**BLOCK DIAGRAM**

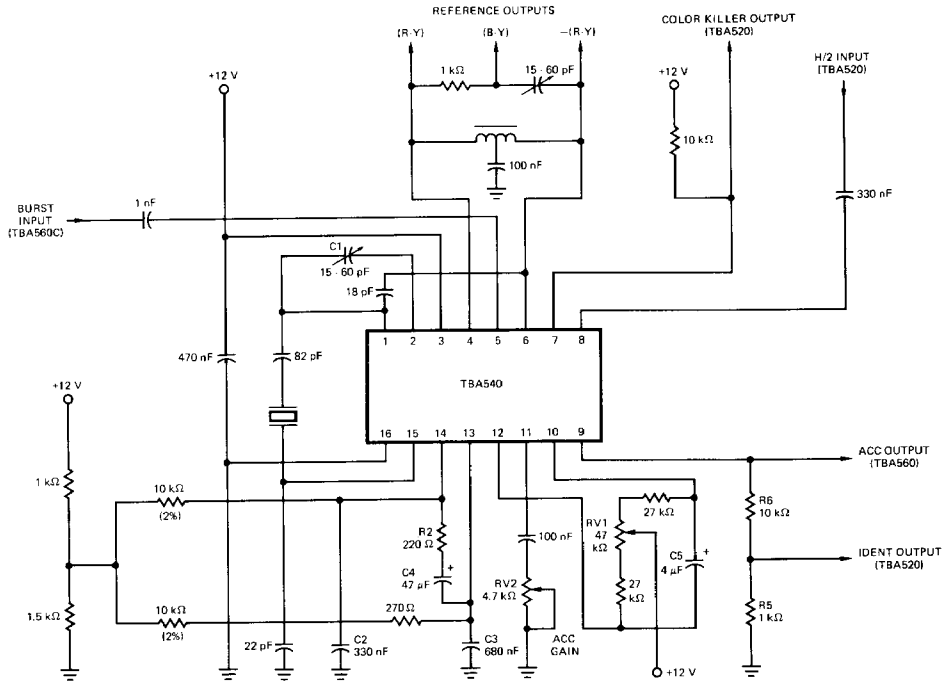



*Planar is a patented Fairchild process.

**ELECTRICAL CHARACTERISTICS:** $V_{3-16}$ = 12 V; $T_A$ = 25°C; $V_{5-16}$ = 1.0 $V_{p-p}$ (burst signal input); $V_{8-16}$ = 2.5 $V_{p-p}$ (PAL Square wave input). Measured in circuit shown in Application Information.

| CHARACTERISTICS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **Output Signals** | | | | | |
| R-Y Reference Signal Output | $V_{4-16}$ | | 1.5 | | $V_{p-p}$ |
| Color Killer Output | | | | | |
| Color On | $V_{7-16}$ | | 12 | | V |
| Color Off | $V_{7-16}$ | | | 250 | mV |
| ACC Output Signal Range | | | | | |
| at Correct Phase of PAL Switch | $V_{9-16}$ | | +4.0 to +0.2 | | V |
| at Incorrect Phase of PAL Switch | $V_{9-16}$ | | +4.0 to +11.0 | | V |
| **Oscillator Section** (Amplifier) | | | | | |
| Input Resistance | $R_{15}$ | | 3.5 | | kΩ |
| Input Capacitance | $C_{15}$ | | 5.0 | | pF |
| Voltage Gain | $V_{15}/V_1$ | | 4.7 | | V/V |
| **Reactance Control Section** | | | | | |
| Voltage Gain with Leads 13 and 14 Interconnected | $V_{15}/V_2$ | | 1.3 | | V/V |
| Rate of Change of Gain $V_{15}/V_2$ with Phase Difference Between Burst and Reference Signal | $\frac{\Delta(V_{15}/V_2)}{\Delta(\phi_5 - \phi_4)}$ | | 5.0 | | $\frac{1}{\text{rad}}$ |
| **Supply Current Consumption** | $I_3$ | | 38 | | mA |

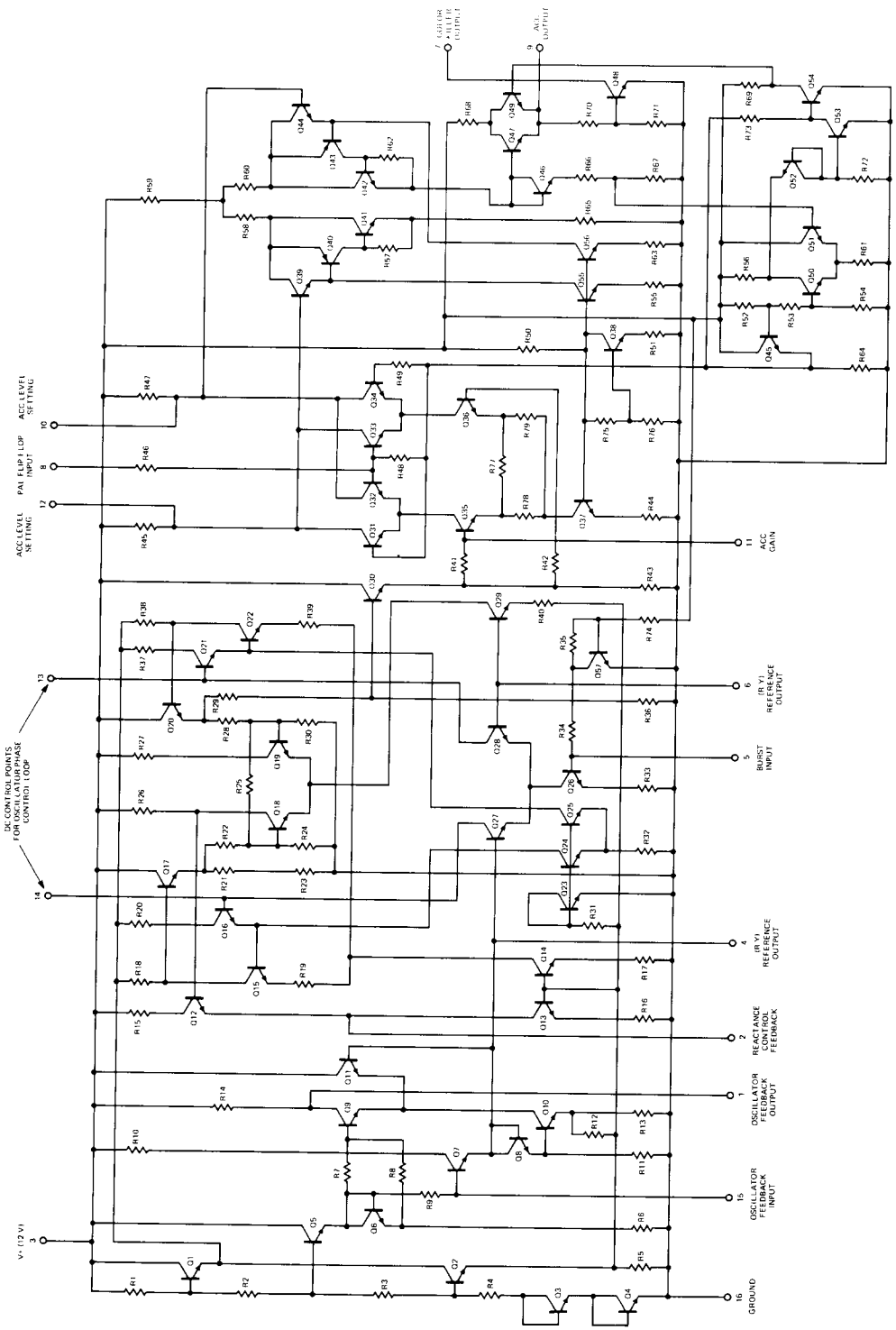
## APPLICATION




### LEAD NAMES

1. Oscillator Feedback Output
2. Reactance Control Stage Feedback
3. Supply Voltage (12 V)
4. Reference Waveform Output (+)
5. Burst Waveform Input
6. Reference Waveform Output (−)
7. Color Killer Output
8. PAL Flip-Flop Square Wave Input
9. ACC Output
10. ACC Level Setting (see also Lead 12)
11. ACC Gain Setting
12. ACC Level Setting (see also Lead 10)
13. DC Control Points for
14. Oscillator Phase Control Loop
15. Oscillator Feedback Input
16. Ground (Negative Supply)

## EQUIVALENT CIRCUIT – TBA540



## APPLICATION INFORMATION

The function is quoted against the corresponding lead number.

1. **Oscillator Feedback Output**
   The crystal receives its energy from this lead. The input impedance is approximately 2 kΩ in parallel with 5 pF.
2. **Reactance Control Stage Feedback**
   This lead is fed internally with a sinewave derived from the reference input (lead 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from lead 2 to the crystal via C1 is such that the value of C1 is effectively increased. Lead 2 is held internally at a very low impedance, therefore, the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.
3. **Positive 12 V Supply**
   The maximum voltage must not exceed 13.2 V.
4. **Reference Waveform Output**
   This lead is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No dc load to ground is required. A dc connection between leads 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on lead 6, a signal of equal amplitude and opposite phase [-(R-Y)] to that on lead 4. A center tap on the inductor, connected to ground via a dc blocking capacitor, is therefore necessary.
5. **Burst Waveform Input**
   A burst waveform amplitude of 1 V peak-to-peak is required to be ac coupled to this lead. The amplitude of the burst will normally be controlled by the adjustment and operation of the ACC circuit. The input impedance at this lead is approximately 1 kΩ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A dc bias of 400 mV is internally derived for lead 5. The absolute level of the tip of the burst at lead 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions, the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the IC which inhibits the performance of the phase lock loop.
6. **Reference Waveform Output**
   This lead requires a reference waveform in the -(R-Y) phase, derived from lead 4 via a bifilar transformer (see lead 4), to drive the internal balanced reactance control stage. A dc connection between leads 4 and 6 must be made via the transformer.
7. **Color Killer Output**
   This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 kΩ) connected to +12 V. The unkilled and killed voltages on this lead are then +12 V and < 250 mV respectively. (The voltage on lead 9 at which switching of the color killer output on lead 7 occurs is nominally +2.5 V.)
8. **PAL Flip-Flop Square Wave Input**
   A 2.5 V peak-to-peak square wave derived from the PAL flip-flop (in the TBA520 demodulator IC) is required at this lead, ac coupled via a capacitor. The input impedance is about 3.3 kΩ.
9. **ACC Output**
   An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal, the dc potential produced at lead 9 is set to be +4 V (RV1). The appearance of a burst signal on lead 5 will cause the potential on lead 9 to go in a negative direction in the event that the PAL flip-flop is identified to be in the correct phase. The range of potential over which full ACC control is exercised at lead 9 is determined by the control characteristics of the ACC amplifier (i.e. for the TBA560C from 1 V to 0.2 V). The potential at lead 9 will fall to a value within this range as the burst input signal is stabilized at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the PAL flip-flop phase is wrong, the potential on lead 9 will move positively. The potential divider R5, R6 will then operate a PAL switch cutoff function in the TBA520 demodulator IC. The switching of the color killer output at lead 7 is designed to occur as the potential on lead 9 moves past +2.5 V.
10. **ACC Level Setting**
    The network connected between leads 10 and 12 balances the ACC circuit and RV1 is adjusted to give +4 on lead 9 with no burst input signal to lead 5. C5 provides filtering.
11. **ACC Gain Control**
    RV2 is adjusted to give the correct amplitude of burst signal on lead 5 (1.5 V peak-to-peak) under ACC control.
12. See lead 10.
13. See lead 14.
14. **DC Control Points in Reference Control Loop**
    Leads 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes of dc balancing the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R2, C2, R3, C3, and R4, C4. The dc potentials on these leads are nominally +7.2 V.
15. **Oscillator Feedback Input**
    The input impedance at this lead is nominally 3.5 k in parallel with 5 pF. No dc connection is required on this lead. The signal voltage ratio in the IC between lead 15 and lead 1 is nominally 4.7 times.
16. **Negative Supply (Ground)**

### PERFORMANCE AND COMMENTS

**Initial Adjustment**

(a) Remove burst signal.
(b) Short circuit leads 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.
(c) Set the ACC level adjustment RV1, to give +4 V on lead 9.
(d) Apply burst signal.
(e) Adjust ACC gain, RV2, to give a burst amplitude of 1.5 V peak-to-peak on lead 5.

**Phase Lock Loop Performance**

(a) Phase difference between reference and burst signals for ±400 Hz deviation of crystal frequency, ±10°.
(b) Typical holding range, ±600 Hz.
(c) Typical pull in range, ±300 Hz.
(d) Temperature coefficient of oscillator frequency, IC only, 2 Hz/°C.