LINEAR INTEGRATED CIRCUITS

L201 L202
L203 L204

HIGH-VOLTAGE, HIGH-CURRENT 7 DARLINGTON ARRAYS

These high-voltage, high-current Darlington transistor arrays comprise seven NPN Darlington pairs on a common monolithic substrate. All units feature open collector outputs and integral suppression diodes for inductive loads. Peak currents of 600 mA can be withstood, making them ideal for driving tungsten filament lamps.
The L 201 is a general-purpose array wich may be used with DTL, TTL, PMOS, CMOS, etc. It is pinned with inputs opposite outputs to facilitate circuit board layout and is priced to compete directly with discrete transistor alternatives.
The L 202 was specifically designed for use with 14 to 25V PMOS devices.
Each input has a Zener diode and resistor in series in order to limit the input current to a safe value.
The L203 has a series base resistor to each Darlington pair allowing operation directly with TTL or CMOS operating at a supply voltage of 5V.
The L204 has a series base resistor to each Darlington pair, allowing operation directly with PMOS or CMOS utilizing supply voltage of 6 to 15V.
In all cases, the individual Darlington pair collector current rating is 500 mA. However, outputs may be paralleled for higher load current capability. The devices are supplied in a 16-lead dual in-line plastic package with copper frame.

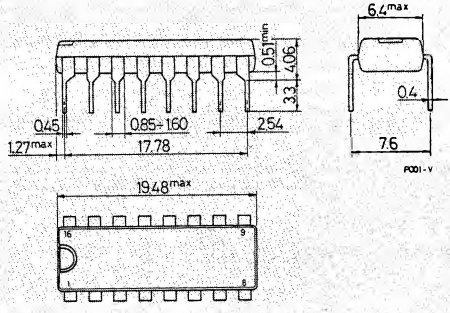
ABSOLUTE MAXIMUM RATINGS

V_i	Input voltage (for **L 202, L 203** and **L 204**)	30	V
V_o	Output voltage (collector-emitter)	50	V
$V_{CEO(sus)}$	Collector-emitter sustaining voltage	36	V
I_C	Collector current	500	mA
I_B	Base current (for **L 201** only)	25	mA
P_{tot}	Total power dissipation at T_{amb} = 25°C	1.8	W
T_{op}	Operating junction temperature	-25 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

ORDERING NUMBERS: L201B, L203B
L202B, L204B

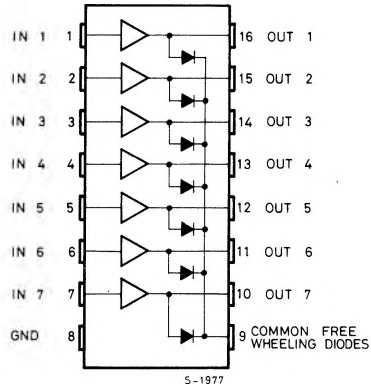
MECHANICAL DATA

Dimensions in mm



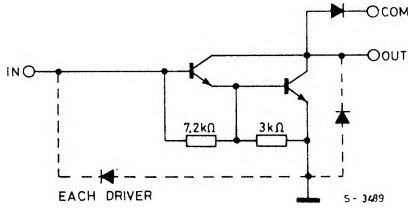
L201 L202 L203 L204

CONNECTION DIAGRAM (top view)

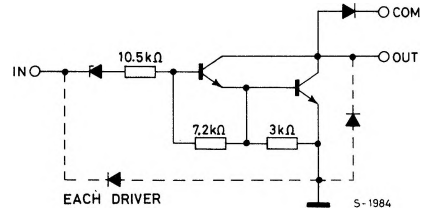


SCHEMATIC DIAGRAM

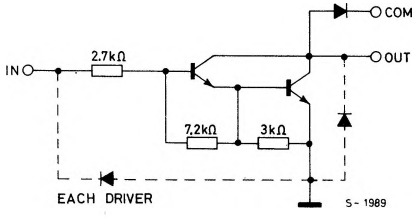
For L 201



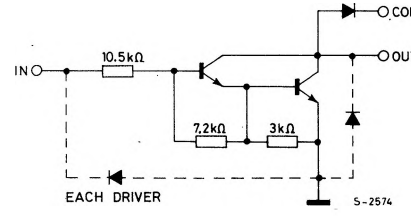
For L 202



For L 203



For L 204



THERMAL DATA

$R_{th\ j\text{-}amb}$	Thermal resistance junction-ambient	max.	70	°C/W

ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, unless otherwise specified)

Parameter		Test conditions	Min.	Typ.	Max.	Unit	Fig. No.
I_{CEX}	Collector cutoff current	for **L 201** V_{CE} = 50V		0.2	3	μA	1
		for **L 202** V_{CE} = 50V V_i = 7V		0.2	3	μA	2
		for **L 203, L 204** V_{CE} = 50V I_i = 0		0.2	3	μA	1
$V_{CE(sat)}$	Collector-emitter saturation voltage	I_C = 350 mA I_B = 500 μA I_C = 200 mA I_B = 350 μA I_C = 100 mA I_B = 250 μA		1.25 1 0.85	1.6 1.3 1.1	V V V	3
I_i	Input current	for **L 202** V_i = 17V		0.75	1.3	mA	
		for **L 203** V_i = 3.85V		0.9	1.35	mA	5
		for **L 204** V_i = 5V V_i = 12V		0.35 1.1	0.5 1.45	mA mA	
$I_{C(off)}$		V_{CE} = 50V I_i = 25 μA			25	μA	4
V_i	Input voltage	for **L 202** I_C = 300 mA V_{CE} = 2V		10.5	13	V	
		for **L 203** I_C = 300 mA V_{CE} = 2V I_C = 250 mA V_{CE} = 2V		1.8 1.7	3 2.4	V V	7
		for **L 204** V_{CE} = 2V I_C = 200 mA V_{CE} = 2V I_C = 350 mA		4.5 5	6 8	V V	
h_{FE}	DC current gain (for **L 201** only)	I_C = 350 mA V_{CE} = 2V	1000	3000		–	3
I_R	Parallel diode reverse current	V_R = 50V		0.5	50	μA	6
V_F	Parallel diode forward voltage	I_F = 350 mA		1.4	2	V	8
t_{PLH}	Turn-on delay time	0.5 V_i to 0.5 V_o			5	μs	–
t_{PHL}	Turn-off delay time	0.5 V_i to 0.5 V_o			5	μs	–

TEST CIRCUITS

Fig 1 - For L 201, L 203 and L 204

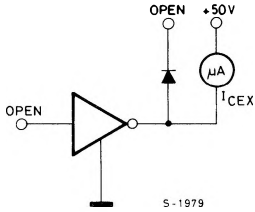


Fig. 2 - For L 202

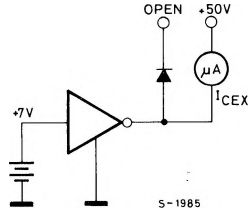


Fig. 3 - For L 201, L 202, L 203 and L 204

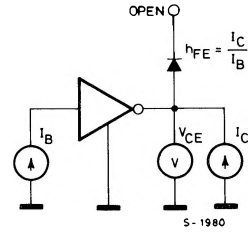


Fig. 4 - For L 201, L 202, L 203 and L 204

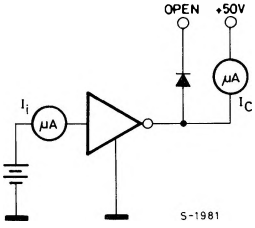


Fig. 5 - For L 202, L 203, and L 204

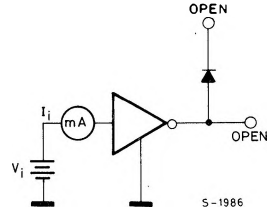


Fig. 6 - For L 201, L 202, L 203 and L 204

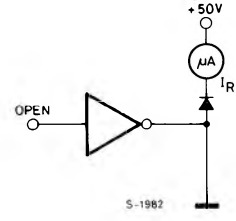


Fig. 7 - For L 202, L 203, and L 204

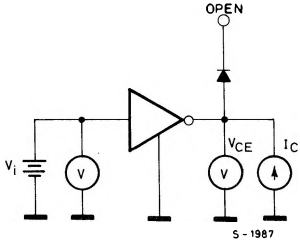
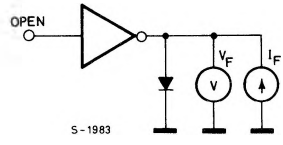
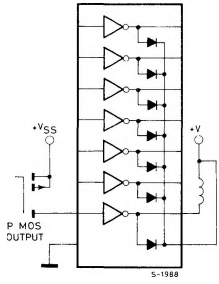


Fig. 8 - For L 201, L 202, L 203 and L 204

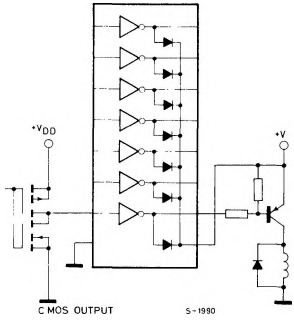


APPLICATION CIRCUITS

PMOS to load
(L 202 and L 204)



Buffer for high current load
(L 203 and L 204)



TTL to load (L 203)

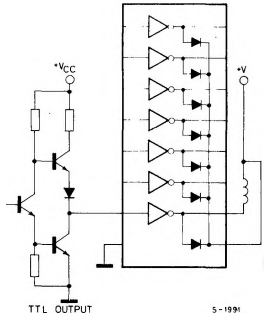


Fig. 9 - DC current gain. vs. collector current (for L 201)

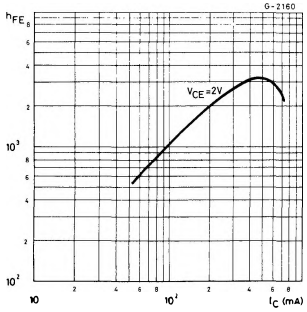


Fig. 10 - Collector current vs. collector emitter saturation voltage

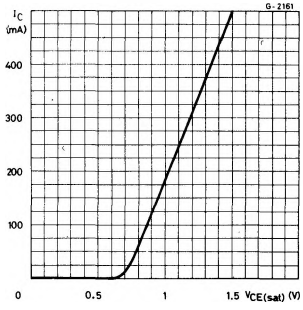


Fig. 11 - Peak collector current as a function fo duty cycle and number of outputs

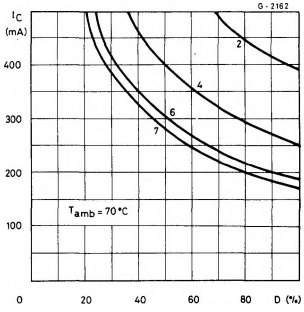


Fig. 12 - Input current vs. input voltage (for L 202 and L 204)

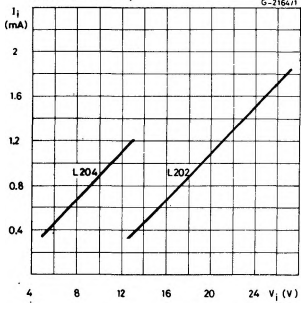


Fig. 13 - Input current vs. input voltage (L 203)

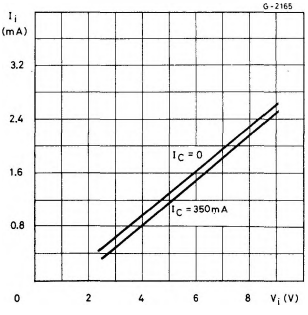


Fig. 14 - Power rating chart