M6M80011AP,L,FP

1024-BIT(64-WORD BY 16-BIT) ELECTRICALLY ERASABLE AND PROGRAMMABLE ROM

DESCRIPTION

The M6M80011AP, L, FP are 1024-bit (64-word x 16-bit) electrically erasable CMOS EEPROMs, and all have a built-in high voltage generator to enable operation in all modes by a single 5V power supply.

The difference between M6M80011AP, M6M80011AL and M6M80011AFP is only outline of package, and the following explanations are for M6M80011AP unless specifically indicated otherwise.

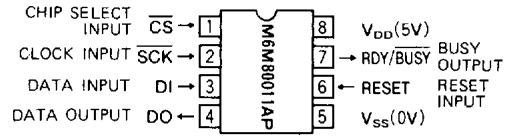
FEATURES

- Single 5V power supply
- Clock synchronous serial I/O
- Three ports control ($\overline{CS}$ and RESET, DI and DO can be interconnected.)
- Built-in sequential controller
- 100000 erase/write cycles
- 10 years data retention

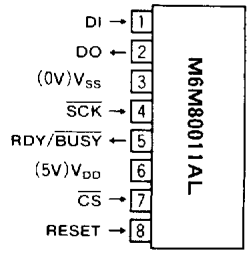
APPLICATION

M6M80011A is especially suitable for use as a nonvolatile channel memory for electronic tuner and as the read only memory system that must be frequently reprogrammed in the field.

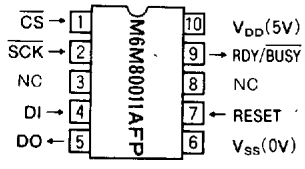
PIN CONFIGURATION (TOP VIEW)



Outline 8P4



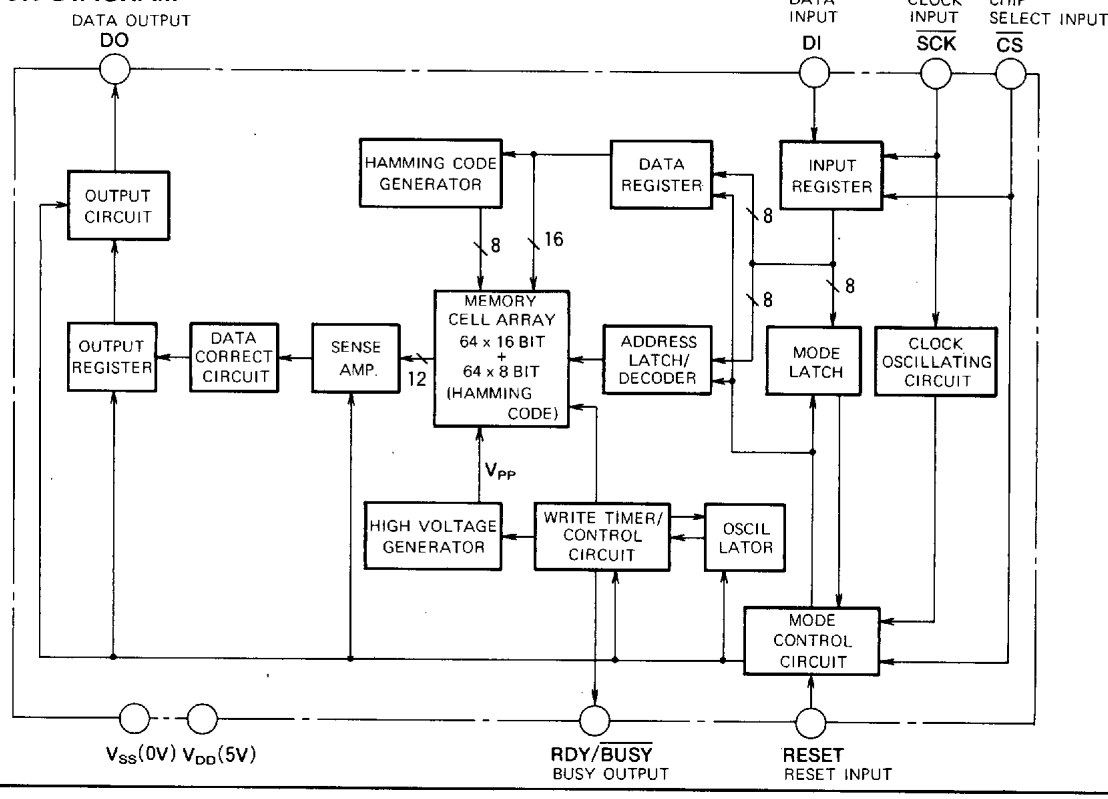
Outline 8P5K



Outline 10P2N-A

NC: NO CONNECTION

BLOCK DIAGRAM



FUNCTIONS

M6M80011AP is a clocked serial port compatible EEPROM, and data is input from the rising edge of clock signal and output by synchronizing to the falling edge of clock signal.

Data is grouped by 8 bits. The beginning 8 bits specify the mode, next 8 bits specify the address, and subsequent 16 bits specify the I/O data.

Any of five modes (write, read, write enable, write disable, status output) may be specified. The write time is set by an internal timer, and determination of whether write operation is in progress or not can be made from status of the RDY/$\overline{BUSY}$ pin or the DO pin status after the status mode has been set.

PIN DESCRIPTION

Pin	Name	Functions
$\overline{CS}$	Chip select input	① Chip selection is made by setting this pin to "L". When this port is "H", the internal sequential controller is reset. Therefore, this pin must be set to "H" before executing each mode. ② During the write operation (when BUSY output is "L"), write operation is continued regardless of the input to this pin. ③ After write operation is finished, this pin must be set to "H" to make mode reading possible. In the case of "status output" mode only, reading is possible even if this pin is "L" after the sequential controller has been reset and t_{STA} has elapsed since the time when the write operation was started.
$\overline{SCK}$	Clock input	① Input data is read at the rising edge of clock. ② Data is output by synchronizing to the falling edge of clock.
DI	Data input	Data is input from this pin.
DO	Data output	Data is output from this pin. DI and DO can be interconnected.
RESET	Reset input	① Must be set to "H" at the time of power ON or OFF. ② When this pin is set to "H", the sequential controller and the write circuit are reset for memory protection. If this pin becomes "H" during write operation, the operation is halted. ③ This pin and $\overline{CS}$ can be interconnected. When this is done, $\overline{CS}$ (=RESET) must be held to "L" during write operation.
RDY/$\overline{BUSY}$	Busy output	① This is "L" during write operation. ② This is "L" at the time of power ON or OFF. In this condition, all inputs are disabled.

MODE FUNCTIONS

Name	Mode	Address	Data	Functions
Read	10101000	$A_0A_1A_2A_3A_4A_500$	$D_0 \sim D_7D_8 \sim D_{15}$	Read from addresses $<A_0 \sim A_5>$
Write	10100100	$A_0A_1A_2A_3A_4A_500$	$D_0 \sim D_7D_8 \sim D_{15}$	Write into addresses $<A_0 \sim A_5>$
Write enable	10100011	XXXXXXXX	——	Write operation is enabled.
Write disable	10100000	XXXXXXXX	——	Write operation is disabled.
Status output	10101001	00XXXXXX	0 (Busy) 1 (Ready)	Busy flag
		10XXXXXX	0 (Enable) 1 (Disable)	Write enable flag
		01XXXXXX	0 (Correct) 1 (Incorrect)	ECC flag

STATUS OUTPUT MODE

(1) Busy flag

The busy flag serves the same function as the $\overline{BUSY}$ output pin.

When this flag is specified, "1" is output when ready from the 16 clock falling edge and "0" is output if busy (write operation in progress).

(2) Write enable flag

M6M80011AP has a write enable flag, and write operation is executed only when this flag is "0". The contents of this flag can be updated only in the write enable (WEN) mode and the write disable (WDS) mode. The contents of this flag is underfined at the power on time, so that the WEN mode must be set before setting the write mode for write operation.

Once the WEN mode is set and this flag is set to the enable state, latch is in effect until the WDS mode is set. EEPROM can be read regardless of the status of this flag.

(3) ECC flag

An ECC circuit, which corrects data errors, is built-in to insure high degree of memory cell reliability. The ECC circuit corrects data errors and outputs the corrected error if there is only one error each in the high-order 8 bits and the low-order 8 bits of 1 word (16 bits). When an error is corrected in at least one of the high-order or low-order byte, this flag is set to "1" to indicate that error correction has been made. The data is corrected in this case. When this flag is "0", it indicates that the correct data value was output without having to active the ECC circuit. By setting the ECC mode after the read mode, ECC information on the address that was specified immediately before can be varified.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Test conditions	Ratings	Unit
V_{DD}	Supply voltage		−0.3~6.0	V
V_I	Input voltage		−0.3~V_{DD}+0.3	V
V_O	Output voltage		−0.3~V_{DD}+0.3	V
$\lvert I_{OH} \rvert$	High-level output current		0~10	mA
I_{OL}	Low-level output current		0~10	mA
T_{stg}	Storage temperature		−40~125	℃
T_{opr}	Operating temperature		−10~70	℃

RECOMMENDED OPERATING CONDITIONS (T_a=−10~70℃, V_{DD}=5V±10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage DI	0.7V_{DD}	V_{DD}	V_{DD}	V
V_{IH}	High-level input voltage RESET, $\overline{CS}$, $\overline{SCK}$	0.8V_{DD}	V_{DD}	V_{DD}	V
V_{IL}	Low-level input voltage DI	0	0	0.3V_{DD}	V
V_{IL}	Low-level input voltage RESET, $\overline{CS}$, $\overline{SCK}$	0	0	0.2V_{DD}	V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{DD}	Supply voltage		4.5	5.0	5.5	V
I_{DD}	Supply current	V_{DD}=5.5V		5	8	mA
V_{IH}	High-level input voltage DI		0.7V_{DD}		V_{DD}	V
V_{IH}	High-level input voltage RESET, $\overline{CS}$, $\overline{SCK}$		0.8V_{DD}		V_{DD}	V
V_{IL}	Low-level input voltage DI		0		0.3V_{DD}	V
V_{IL}	Low-level input voltage RESET, $\overline{CS}$, $\overline{SCK}$		0		0.2V_{DD}	V
V_{OH}	High-level output voltage	I_{OH}=−400μA	2.4			V
V_{OL}	Low-level output voltage	I_{OL}=2.1mA			0.4	V

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t_{WH}	Positive data shift clock pulse width		450			ns
t_{WL}	Negative clock pulse width		450			ns
t_{WWH}	Clock hold time (every 8 clocks)		4			μs
$t_{su(CS-SCK)}$	Chip select set up time before the fall of the clock		1			μs
$t_{h(SCK-CS)}$	Chip select hold time after the rise of the clock		4			μs
$t_{su(DI-SCK)}$	Data set up time before the rise of the clock		150			ns
$t_{h(SCK-DI)}$	Data hold time after the rise of the clock		200			ns
$t_{su(SCK-CS)}$	Clock set up time before the fall of the chip select		1			μs
$t_{h(CS-SCK)}$	Clock hold time after the rise of the chip select		1			μs
t_{PD}	Data delay time after the fall of the clock				350	ns
t_{dv}	Data valid time after the rise of the chip select				1	μs
$t_{E/W}$	Self-time write sequence time				15	ms
t_{CSH}	Positive chip select width		4			μs
t_{hw}	Chip select, clock hold time after the start of the write sequence		4			μs
t_{STA} (Note 1)	At setting status mode, clock hold time start of the write sequence when CS is 0.		12			μs

Note 1. t_{STA} indicates the maximum value of the sequential controller reset pulse that is generated after the write operation is started. When the sequential controller is reset, only the status output can be read.

NONVOLATILE CHARACTERISTICS

Symbol	Parameter	Test conditions	Limits			Units
			Min	Typ	Max	
N_{EW}	Erase/Write cycle per word		10^5			cycles
t_S	Data retention	$N_{EW}=10^5$	10			years

TIMING DIAGRAMS

(1) Synchronizing data I/O timing

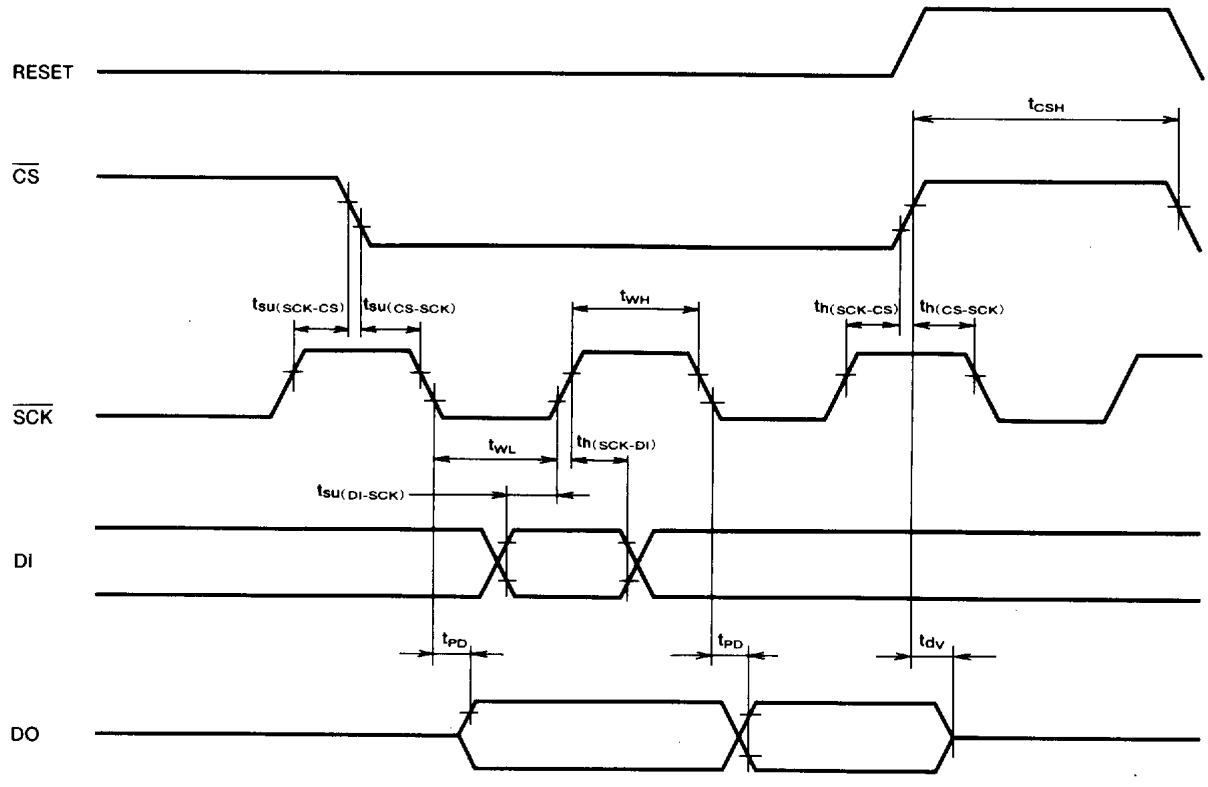


Fig. 1 Synchronizing timing

(2) $\overline{SCK}$ "H" hold time at every 8 clocks

The timing pattern shown above is maintained during transfer of 8-bit data, but the clock "H" hold time t_{wwh} is necessary at every 8th clock for $\overline{SCK}$ input in all modes.

TIMING CHART for VARIOUS MODES

(1) When controlling $\overline{CS}$ and RESET pins

- **Write enable and write disable mode**

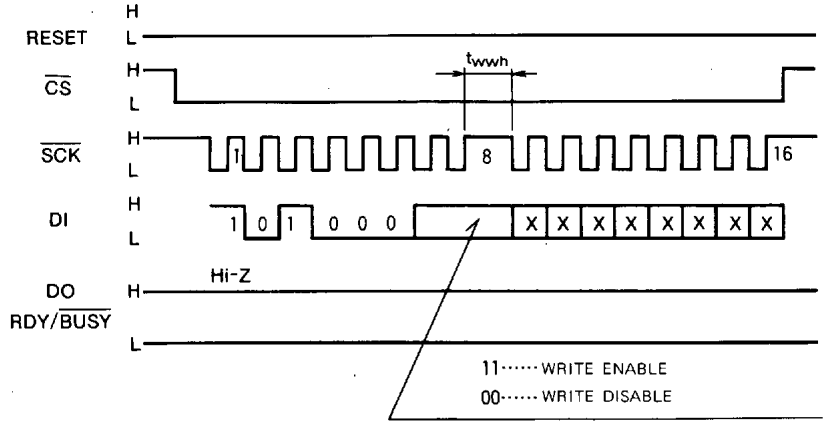


Fig. 2 Sequence at write enable and write disable modes

- **Status output mode**

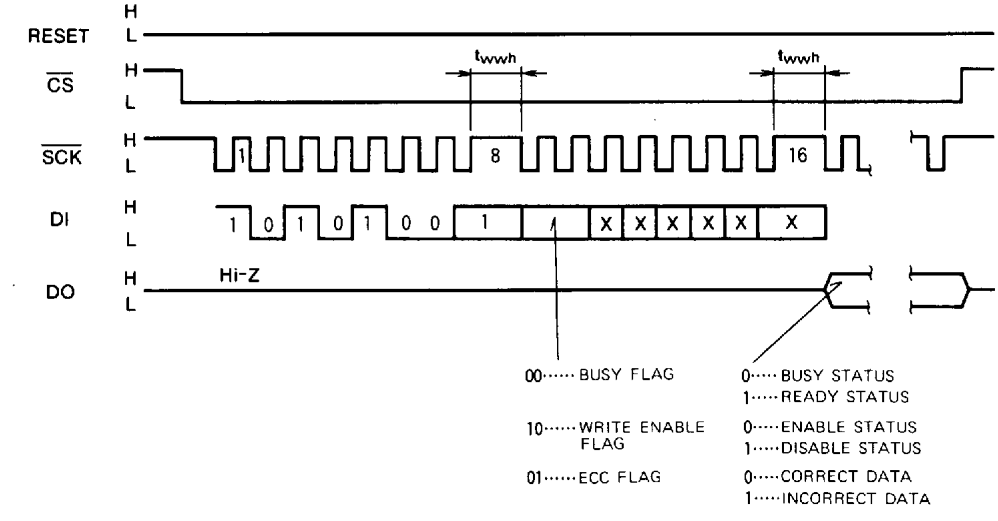


Fig. 3 Sequence at status output mode

The status of each status flag specified from the DO pin is output starting at the rising edge of the 16th clock. Output is not dependent on clock but continues until $\overline{CS}$ becomes "H".

- **Read mode**

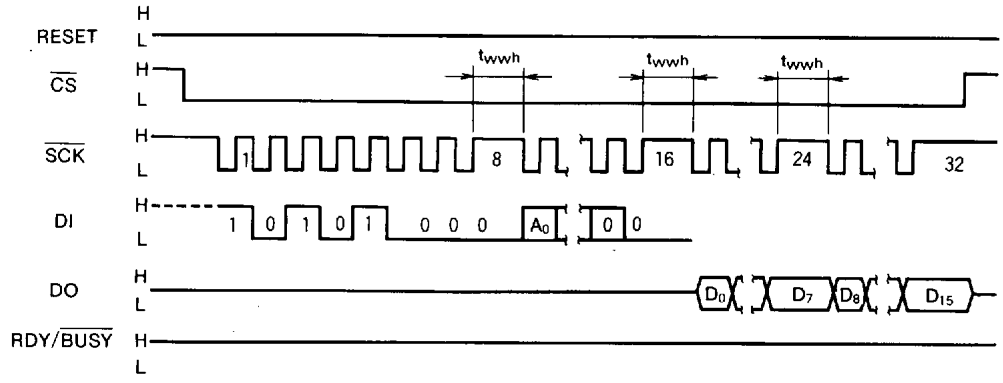


Fig. 4 Sequence at read mode

- **Write mode**

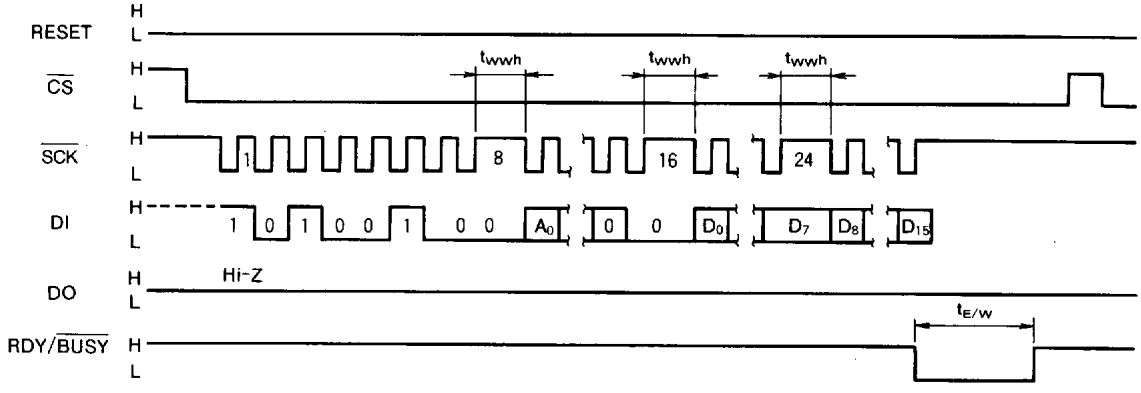


Fig. 5 Sequence at write mode

Execution of the write operation starts at the rising edge of the 32nd clock.

During the write operation, the $\overline{CS}$ input value may be either "H" or "L". If the $\overline{CS}$ pin is held to "L" during the write operation, the read operation is possible only in the status mode.

Thus, the $\overline{SCK}$ is to be used for other tasks during the write operation, $\overline{CS}$ should be set to "H" as shown in Figure 6 (even is $\overline{CS}$ is held to "L", $\overline{SCK}$ can be used by other tasks if a dummy bit input is performed as shown in Figure 10).

To read next mode after $t_{E/W}$, $\overline{CS}$ must be set to "H" first.

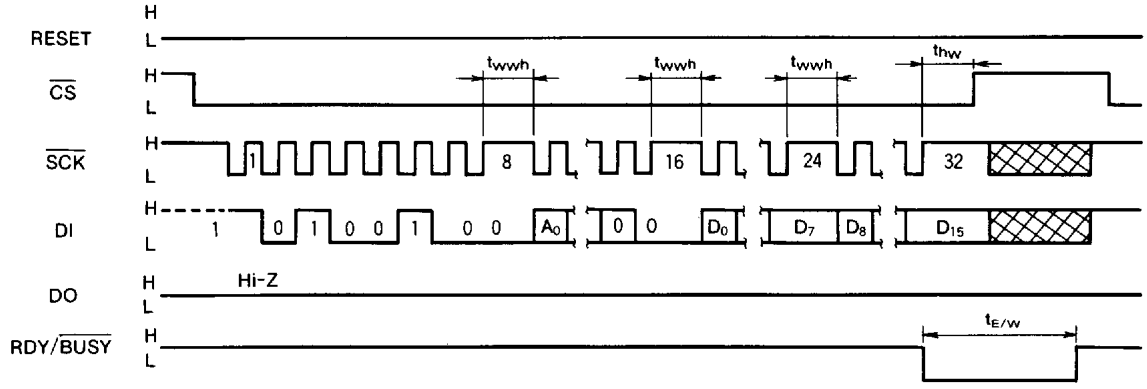


Fig. 6 Sequence at write mode

To use $\overline{SCK}$ and DI for other tasks during the write operation, $\overline{CS}$ must be set to "H" after t_{hw} has elapsed from the rising edge of the 32nd clock as shown in Figure 6.

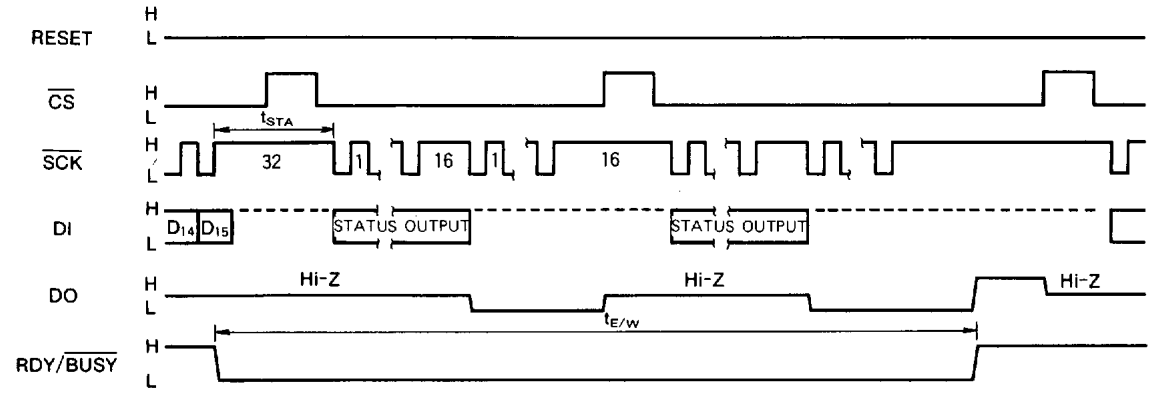


Fig. 7 Sequence of status output (busy flag) during the write operation

After write operation has started, the sequential controller is reset automatically, so read operation in the status mode become possible only after t_{STA} has elapsed from the time the write operation started without having to set $\overline{CS}$ to "H".

Before the status mode is set again, $\overline{CS}$ must be set to "H" as in the ordinary mode setting procedure.

(2) When connecting between $\overline{CS}$ and RESET pins

- **Write mode**

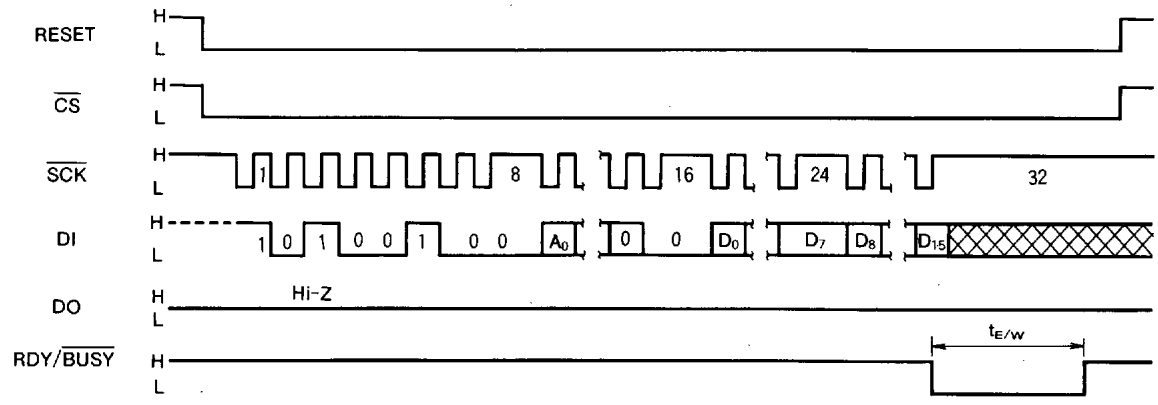


Fig. 8 Sequence of write operation

During the write operation, the $\overline{CS}$=RESET pin must be set to "L".

Because the read operation is possible only in the status mode once the write operation starts as described above, $\overline{SCK}$ must be held to "H" when not setting the status mode. For using $\overline{SCK}$ and DI for other tasks during the write operation, see Figure. 10.

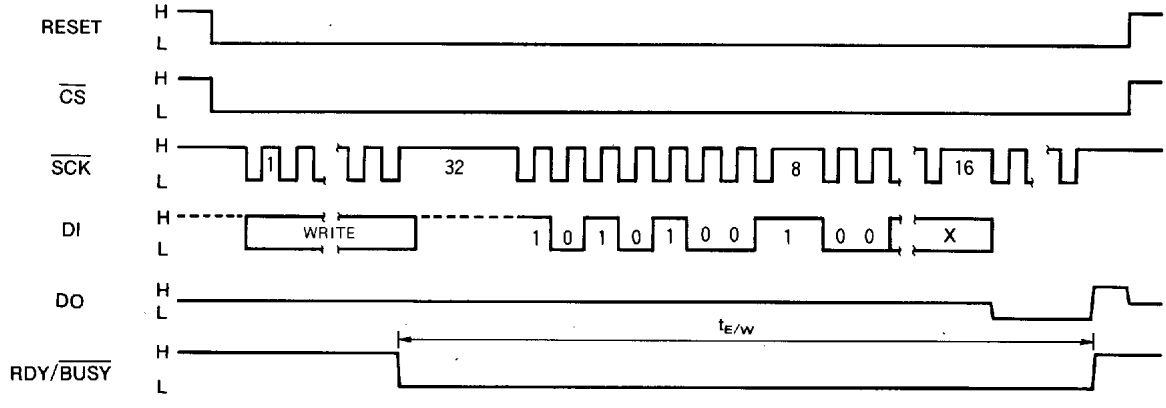


Fig. 9 Sequence of status output during write operation

The read operation in the status mode becomes possible after t_{STA} has elapsed from the time the write operation started. Attention is called to the fact, when the status mode is set, the DO pin is in the output state until $\overline{CS}$ is set to "H".

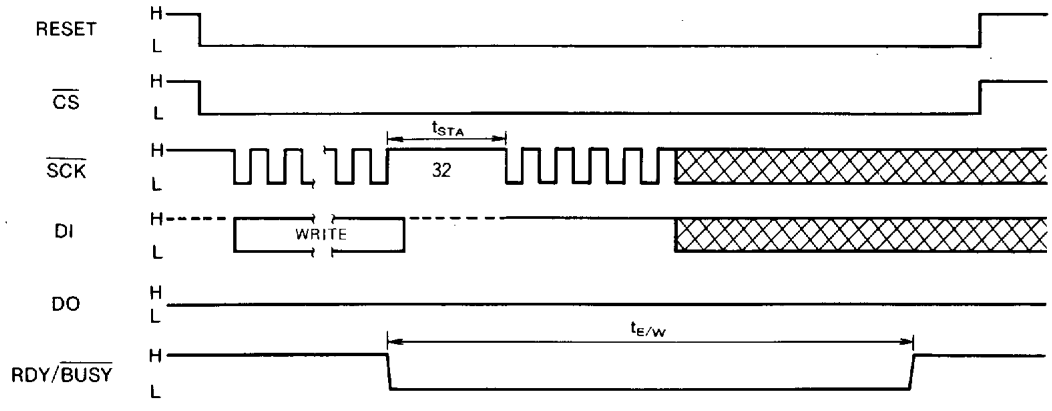


Fig. 10 Sequence of write operation

As shown in Figure 9, the read operation in the status mode becomes possible after t_{STA} has elapsed from the time the write operation started, and the DO pin is set to the output state when the status mode is set. When using the DO pin is addition to the $\overline{SCK}$ and DI pins for other tasks, a dummy bit input must be made after t_{STA} has elapsed from the time the write operation started to avoid the status mode before executing the other tasks.

Other (than dummy bit) data input is equally effective for this purpose as long as it does not generate the status mode instruction code (10101001).