FAIRCHILD SEMICONDUCTOR™

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DM74S74
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear, and Complementary Outputs

General Description

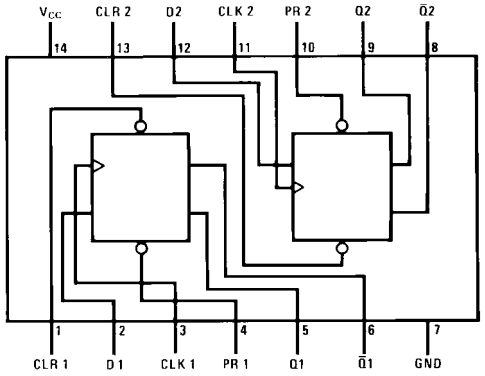
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM74S74M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74S74N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
* = This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to its inactive (HIGH) level.
Q_0 = The output logic level of Q before the indicated input conditions were established.

Absolute Maximum Ratings(Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		Min	Nom	Max	Units
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage		2			V
V_{IL}	LOW Level Input Voltage				0.8	V
I_{OH}	HIGH Level Output Current				−1	mA
I_{OL}	LOW Level Output Current				20	mA
f_{CLK}	Clock Frequency (Note 2)		0	110	75	MHz
f_{CLK}	Clock Frequency (Note 3)		0	95	65	MHz
t_W	Pulse Width (Note 2)	Clock HIGH	6			ns
		Clock LOW	7.3			
		Clear LOW	7			
		Preset LOW	7			
t_W	Pulse Width (Note 3)	Clock HIGH	8			ns
		Clock LOW	9			
		Clear LOW	9			
		Preset LOW	9			
t_{SU}	Setup Time (Note 2)(Note 4)		3↑			ns
t_{SU}	Setup Time (Note 3)(Note 4)		3↑			ns
t_H	Input Hold Time (Note 2)(Note 4)		2↑			ns
t_H	Input Hold Time (Note 3)(Note 4)		2↑			ns
T_A	Free Air Operating Temperature		0		70	°C

Note 2: C_L = 15 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 3: C_L = 50 pF, R_L = 280Ω, T_A = 25°C and V_{CC} = 5V.

Note 4: The symbol (↑) indicates the rising edge at the clock pulse is used for reference.

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 5)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = – 18 mA				–1.2	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.7	3.4		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.5	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max V_I = 2.7V	D			50	µA
			Clear			150	
			Preset			100	
			Clock			100	
I_{IL}	LOW Level Input Current	V_{CC} = Max V_I = 0.5V (Note 6)	D			–2	mA
			Clear			–6	
			Preset			–4	
			Clock			–4	
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 7)		–40		–100	mA
I_{CC}	Supply Current	V_{CC} = Max, (Note 8)			30	50	mA

Note 5: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 6: Clear is tested with preset HIGH and preset is tested with clear HIGH.

Note 7: Not more than one output should be shorted at a time, and the duration should not exceed one second.

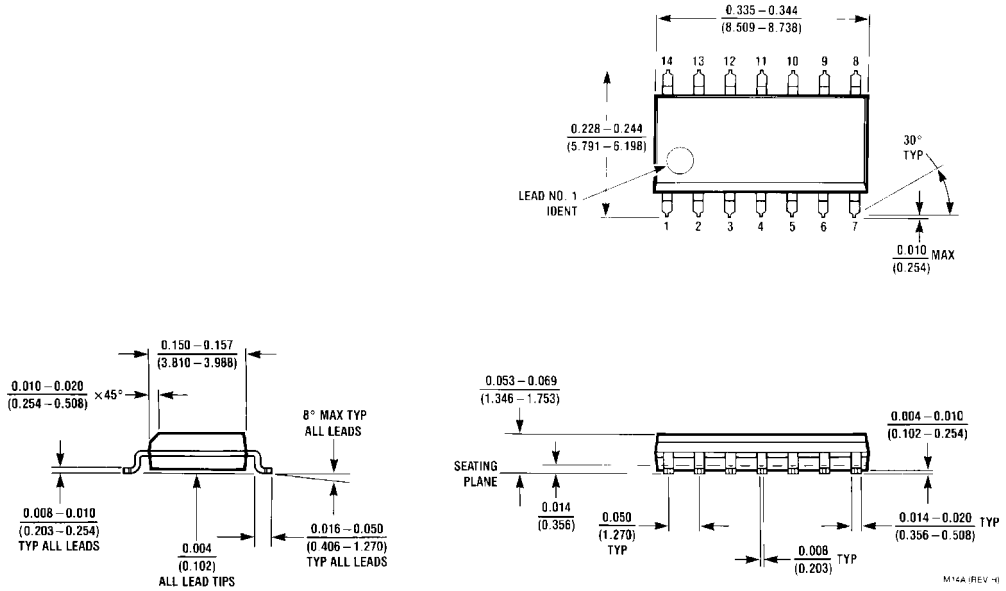
Note 8: With all outputs OPEN, I_{CC} is measured with the Q and $\overline{Q}$ outputs HIGH in turn. At the time of measurement, the clock is grounded.

Switching Characteristics

at V_{CC} = 5V and T_A = 25°C

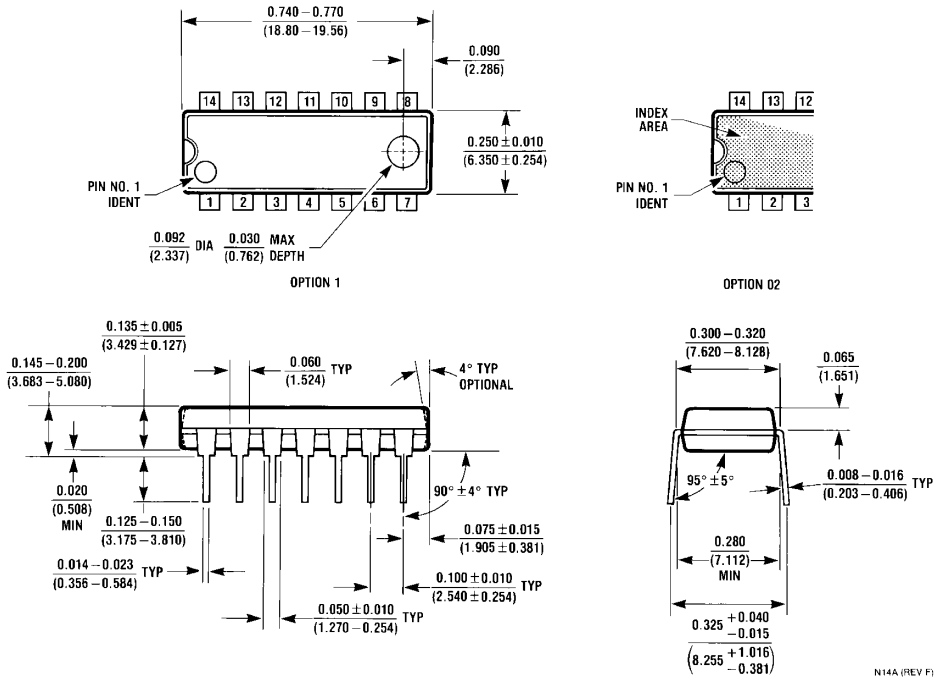
Symbol	Parameter	From (Input) To (Output)	R_L = 280Ω				Units
			C_L = 15 pF		C_L = 50 pF		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency		75		65		MHz
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		6		9	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clear to $\overline{Q}$		6		9	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (Clock HIGH)	Preset to $\overline{Q}$		13.5		17	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (Clock LOW)	Preset to $\overline{Q}$		8		14	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (Clock HIGH)	Clear to Q		13.5		16	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output (Clock LOW)	Clear to Q		8		13	ns
t_{PLH}	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or $\overline{Q}$		9		12	ns
t_{PHL}	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or $\overline{Q}$		9		14	ns

Physical Dimensions inches (millimeters) unless otherwise noted



14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N14A