MOTOROLA
Semiconductors
BOX 20912 • PHOENIX, ARIZONA 85036

MC14507

QUAD EXCLUSIVE "OR" GATE

The MC14507 quad exclusive OR gate is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

- Quiescent Current = 0.5 nA/package typical @ 5 Vdc
- Noise Immunity = 45% of V_{DD} typical
- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Single Supply Operation – Positive or Negative
- High Fanout >50
- Input Impedance = 10^{12} ohms typical
- Logic Swing Independent of Fanout

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

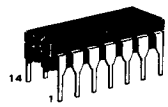
NOTE:

Not Recommended for New Designs. Use MC14070B as a Direct Replacement.

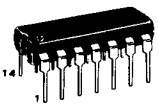
McMOS SSI

(LOW-POWER COMPLEMENTARY MOS)

QUAD EXCLUSIVE "OR" GATE



L SUFFIX
CERAMIC PACKAGE
CASE 632

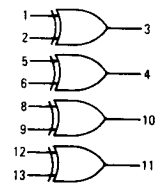


P SUFFIX
PLASTIC PACKAGE
CASE 646

ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

LOGIC DIAGRAM
POSITIVE LOGIC



3 = 1⊕2

V_{DD} = Pin 14
V_{SS} = Pin 7

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