monolithic dual n-channel JFETs *designed for . . .*

Siliconix

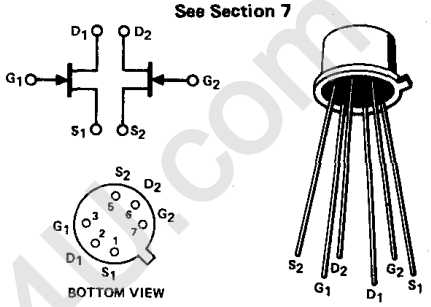
Performance Curves NNR See Section 5

■ High Gain Differential Amplifiers

BENEFITS

- Minimum System Error and Calibration
  5 mV Offset Maximum (2N5045)
- Low Drift
  5 mV Drift Maximum (2N5045)

TO-71
See Section 7



*ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage . . . . . -50 V
Forward Gate Current . . . . . 30 mA
Total Dissipation (25°C Free Air Temp.) . . . . . 400 mW
Power Derating (to 175°C) . . . . . 2.67 mW/°C
Storage Temperature Range . . . . . -65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) . . . . . 300°C

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic (Note 1)		2N5045		2N5046		2N5047		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max			
1	STATIC	I_{GSS}	Gate Reverse Current		-1		-1		-1	μA	V_{GS} = -50 V, V_{DS} = 0 V	
2					-0.25		-0.25		-0.25	nA	V_{GS} = -30 V, V_{DS} = 0 V	
3					-250		-250		-250			T = 150°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.5	-4.5	-0.5	-4.5	-0.5	-4.5	V	V_{DS} = 15 V, I_D = 0.5 nA	
5		I_{DSS}	Drain Saturation Current	0.5	8.0	0.5	8.0	0.5	8.0	mA		
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	1.5	6.0	1.5	6.0	1.5	6.0	mmho	V_{DS} = 15 V, V_{GS} = 0 V	f = 1 kHz
7		$\lvert y_{fs} \rvert$	Common-Source Forward Admittance	1.5		1.5		1.5				f = 100 MHz
8		g_{os}	Common-Source Output Conductance		25		25		25	μmho		f = 1 kHz
9		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0	pF		f = 1 MHz
10		C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
11		NF	Spot Noise Figure		5.0		5.0			dB		f = 10 Hz, R_G = 1 MΩ
12		$\bar{e}_n$	Equivalent Short-Circuit Input Noise Voltage		200		200			$\frac{nV}{\sqrt{Hz}}$		f = 10 Hz
13	MATCHING	$\lvert I_{GSS1} - I_{GSS2} \rvert$	Differential Gate Current		10		10		10	nA	V_{GS} = -15 V, V_{DS} = 0 V	T_A = 100°C
14		I_{DSS1}/I_{DSS2}	Drain Current Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{GS} = 0 V, V_{DS} = 15 V	
15		$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DS} = 15 V	I_D = 50 μA
16					5		10		15			I_D = 200 μA
17		$\lvert \Delta \lvert V_{GS1} - V_{GS2} \rvert \rvert$	Gate-Source Voltage Differential Drift (Note 3)		5		10		15		V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C	T_B = -25°C
18					5		10		15			T_B = 100°C
19		$\lvert g_{fs1}/g_{fs2} \rvert$	Transconductance Ratio (Note 2)	0.95	1.0	0.9	1.0	0.8	1.0	—	V_{DS} = 15 V, I_D = 200 μA	f = 1 kHz
20		$\lvert g_{os1} - g_{os2} \rvert$	Diff. Output Conductance		1.0		2.0		3.0	μmho		

*JEDEC registered data.

NOTES:
1. Individual FET characteristics. The terminals of the FET not under test are open-circuited for these measurements..
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

NNR
NRL-D